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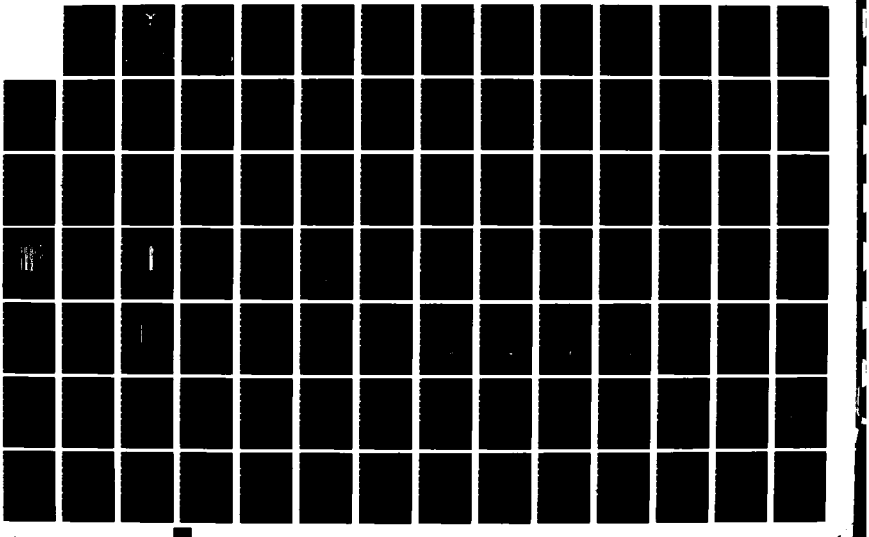

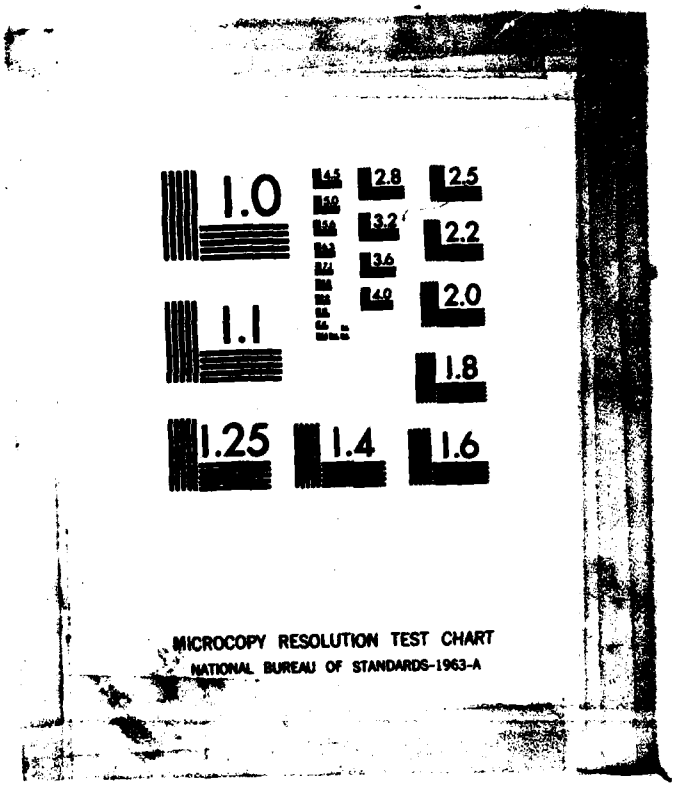
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DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY (ATC)

AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

S-BAND VARIABLE TIME DELAY CIRCUIT

ON BARIUM TETRATITANATE

THESIS

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S-BAND VARIABLE TIME DELAY CIRCUIT ON BARIUM TETRATITANATE

THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

in Partial Fulfillment of the

Requirements for the Degree of

Master of Science

by

Robert F. Bellacicco

2nd Lt USAF

Graduate Electrical Engineering

December 1982

Preface

Through this project a design for a ½ to 8 nsec time delay circuit was developed. My original intent was to fabricate this circuit on $BaTi_4O_9$ and test it. However, all attempts to process the substrates through published fabrication techniques proved to be futile. Therefore my work was halted at the design stage.

During my thesis work, the efforts of several people helped to make this such a successful learning experience for me. My appreciation goes out to Larry Horn and Larry Calahan for their assistance in circuit fabrication, to Marc Calcattera and Roger Colvin for helping me in understanding the black art of microwave circuitry, and to Carl Shorte and his craftsmen at the AFIT machine shop. A special thanks is due to my wife, Lori, for her patience and understanding.

ROBERT F. BELLACICCO

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List of Symbols

ANA	automatic network analyzer
C	capacitance
DUT	device under test
E_I	incident voltage
E_O	initial voltage
E_R	reference voltage
E_{RL}	reflected voltage
E_T	test channel voltage
h	microstrip substrate thickness
L	inductance
L_R	reference channel length
L_T	test channel length
NA	network analyzer
R	resistance
s	microstrip line separation
t	microstrip line thickness
TDU	time delay unit
v_m	signal velocity in microstrip line
v_o	signal velocity in air
VSWR	voltage standing wave ratio
w	microstrip line width
X_C	capacitive reactance
X_L	inductive reactance
Z_o	characteristic impedance of a line

List of Symbols (cont.)

β	phase constant
ϵ_R	relative, dielectric constand
ϵ_{RE}	effective relative dielectric constant
λ_m	wavelength in microstrip line
λ_o	wavelength in air
ρ	reflection coefficient
τ	time delay
τ_D	time delay difference between τ_R and τ_T
τ_R	time delay in reference channel
τ_T	time delay in test channel
ϕ_D	phase difference between ϕ_T and ϕ_R
ϕ_R	signal phase in reference channel
ϕ_T	signal phase in test channel
ω	angular frequency

Abstract

The performance requirements for a variable time delay circuit for use in a phased array antenna are given - time delay from ½ to 16 nsec, 3 GHz operating frequency, 20% bandwidth, temperature compensation, and compact size. A brief description is presented of various types of devices which could meet these requirements. Mircrostrip device construction was used in this project.

In the research for the electrical structure of this time delay circuit, two design types were investigated. The first, a tapped transmission line, yielded poor results on a test circuit - high insertion loss (2-22 db) and high VSWR. The second design was that of a 5-bit network. Test circuit results showed this to be a relatively good design - insertion loss of 0.7 - 5.0 db and VSWR of 1.8 to 2.5.

A complete time delay circuit design was produced using a 4-bit structure for the RF transmission line (½ to 8 nsec in ½ nsec increments) and a loaded switched-line structure for selection of the amount of time delay. For temperature compensation, the circuit design was dimensioned for a ~~$BaTi_4O_9$~~ barium tetratitinate microstrip substrate. Due to small substrate size, the maximum time delay was 8 nsec instead of 16 nsec.

S-BAND VARIABLE TIME DELAY CIRCUIT ON BARIUM TETRATITANATE

I. Introduction

Background

Definition of Time Delay Unit. (Ref 22:389-399) In microwave circuitry, where the phase of a signal is as important as its amplitude, a category of devices exists expressly for adjusting phase. These devices are called phase shifters or time delay units (TDU), depending upon their delay characteristics and specific applications.

These devices are typically two port units. The amount of change they introduce to the phase of a signal passing through the device is determined by comparing the voltage phase at the input port (ϕ_1) to the voltage phase at the output port (ϕ_2). If the phase difference ($\Delta\phi$) is less than 360 degrees, the device causing the $\Delta\phi$ is called a phase shifter, and if $\Delta\phi$ is greater than 360 degrees, it is referred to as a time delay unit.

Furthermore, the $\Delta\phi$ of a TDU or a phase shifter is frequency dependent, but the time delay, τ, is frequency independent. Therefore, for clarity the delay characteristic of a TDU is denoted in terms of nanoseconds or microseconds as opposed to degrees or fractions of a wavelength.

Another characteristic of TDUs is that they should affect the amplitude of a signal as little as possible. Low loss, unfortunately, is difficult to achieve. Typical inser-

tion loss for a TDU ranges from one half to several decibels.

In many cases more than one fixed amount of time delay is necessary. This need leads to variable time delay units which allow various amounts of delay to be either electronically or mechanically chosen. This thesis deals with a variable TDU. The design goal is a TDU with a time delay from zero to sixteen nanoseconds in one half nanosecond increments over a 600 MHz bandwidth centered about 3GHz.

Applications of Time Delay Units. (Ref 10:986-990) In this section a few TDU applications will be presented as examples of the different areas in which TDUs are used.

The first application is in electronic countermeasure systems. Variable microwave delay lines are used to "produce false range and speed information." These systems need broad bandwidth, low loss, and a wide range of time delays. A second use for TDUs is radar test equipment. A signal passed through a time delay unit is used to simulate the return from a moving target. "A variable delay range of from one to 150 microseconds" would be needed for this application. Also, losses up to 100 db are acceptable.

A final and perhaps the most important use of a TDU is in phased array radars. (Ref 18:278-280) Variable time delay units provide the means for varying the relative phase of signals transmitted from each element of an array antenna. These relative phase variations allow the generated beam to be steered in a desirable direction. Depending upon the radar system, a TDU for phased array purposes would

need to be broadband, to operate somewhere in the 500 MHz to 10 GHz range, and to have a time delay of up to 100 nanoseconds.

Presently Used Devices. Many different schemes are being used today for time delay devices. A popular and accurate device uses sections of coaxial cable of various lengths. (Ref 21:401) By electronically selecting from these cable sections, different delays are attainable. The problem with this system, though, is that the coaxial cable plus the needed switching network are bulky. In planar phased array antennas composed of thousands of elements and their accompanying drive circuitry, a bulky TDU is very undesirable.

Other types of TDUs use stripline and microstrip design and fabrication techniques. The electrical theory behind these devices is the same as for the device described above which uses coaxial cable. A control unit electronically selects an electrical path from a group of transmission lines printed on a substrate. These different lines yield various values of time delay. Both are compact compared to the coaxial cable device, but they are usually temperature senstive.

Objective

The goal of this project is to design a microwave variable time delay unit. The device is to be broadband, low loss, and have a delay range of zero to sixteen nanoseconds. It will operate with a bandwith of

600 MHz centered about 3 GHz and should be temperature stable. The barium tetratitanate substrate onto which the device is to be fabricated will provide the temperature stabilization. The design should provide a device which is compact and relatively inexpensive to fabricate.

Assumptions

Microstrip design and fabrication techniques were used in this project, and although microstrip is a relatively new procedure, volumes of material are available concerning design equations and fabrication procedures. These equations were assumed to be accurate enough for the purposes of this project.

Also, the specifications for the available substrates were assumed to be correct. Both alumina and barium tetratitanate have been used in the fabrication of microwave devices for many years, and results obtained from both have been documented well enough to justify this assumption.

Scope

Due to time constraints, the scope of this project was limited in two ways. First, keeping the designs relatively simple to fabricate meant only single layer designs could be used. Therefore, chip components such as chip resistors were used instead of printed components.

Secondly, only a limited number of test circuits could be made. These test circuits took several weeks to design, fabricate, and test. Therefore, only two generations of test circuits were used for this project.

Approach

The approach taken for this project was to design a full TDU, select portions of this design to be placed on a test circuit, and perform data measurements on this circuit. Then with this data the initial TDU design was revised, sections of this design were chosen for a second test circuit, and this circuit was fabricated and tested. With the knowledge accumulated from the two test iterations, a full TDU was designed and documented.

Sequence of Presentation

In this report, the detailed specifications given for the device to be designed are presented. Then the theory and equations used for microstrip design are explained. Next, the details of the two test circuits are listed along with the test results for each. This section leads into the design results of the final time delay unit. In the final section, conclusions arrived at while working on this project and recommendations for further work are given.

II. Design Analysis and Theory

The circuit requirements given by this project's sponsor are presented in detail in the beginning of this section. ollowing this is a discussion of the design alternatives available and of why microstrip was chosen. Then the two design philosophies which were researched are explained. The final part of this section explains the theory of microstrip design techniques.

Specifications

The circuit specifications by which this thesis was guided are listed below.

1) Variable Time Delay. Through electronic control, the circuit will allow a user to select time delay ranging from zero to sixteen nanoseconds in one half nanosecond increments.
2) Microwave Operating Frequency. Since the application for the time delay unit is in phased array radar antenna systems, the circuit's operating frequency will be 3 GHz.
3) Broad Band. This term is a relative one, but in this case it is defined as 20 percent. Therefore, the designed circuit will exhibit good characteristics from 2.7 GHz to 3.3 GHz.
4) Low Loss. Like "broadband", this phrase is difficult to define. However, due to the amount of delay desired, losses of 10 to 20 db are expected.

5) Temperature Stable. The designed circuit will show negligible frequency drift and time delay fluctuation due to temperature variations.

6) Compact. The final delay circuit design should fit on a 2 inch by 2 inch substrate.

These requirements admittedly leave much room for interpretation. Ultimately, optimization of performance and minimization of size were used as design goals.

Design Alternatives

At the beginning of this project the use of microstrip design and fabrication techniques was suggested, because the advantages of microstrip for this application, over other available techniques outweighted its disadvantages. This section presents the advantages and disadvantages of waveguide, coaxial cable, stripline, and microstrip time delay units and also of the two available substrates. Table I summarizes the properties of these microwave circuit types.

The electronic configuration used as a standard for this thesis consists of various lengths of transmission line and a switching network. the time delay is selected by electronically switching to cascaded line sections such that the total length corresponds to the desired delay. Details of the layouts and switching networks for the various circuit constructions will not be discussed.

A time delay unit (TDU) incorporating waveguides as its transmission line sections would have extremely good RF characteristics: Low Loss, high Q, high power capability, and very

Table I. Comparison of Popular Microwave Transmission Media. (Ref 3:174)

Characteristic	Microstrip	Stripline	Coaxial	Waveguide
Line Losses	high	high	medium	low
Unloaded Q	low	low	medium	high
Power Capability	low	low	medium	high
Isolation between neighboring circuits	poor	fair	very good	very good
Bandwidth	large	large	large	small
Miniaturization	excellent	very good	poor	poor
Volume and Weight	small	medium	large	large
Realization of passive circuits	very easy	very easy	easy	easy
Integration with chip devices	very good	fair	poor	poor
with ferrites	good	good	poor	good
with lumped elements	very good	very good	good	poor

good isolation from other circuit components. (Ref 3:174) However, a time delay of sixteen nanoseconds would require about eleven feet of waveguide, and thus the TDU would be very bulky. Also, a switching network for waveguide sections by itself is rather large. (Ref 21:361) Because of the requirement for small size for this thesis design, waveguide is obviously not a feasible alternative.

A second design technique which uses coaxial cable would be more compact than the TDU described above since coaxial cable is typically smaller than waveguide and is flexible enough to be packed close together. This coaxial TDU would have relatively good RF characteristics, and its switching network could use small PIN diode switches. Thus, a coaxial TDU could be much smaller than a waveguide unit, but the eleven feet of coaxial cable required for sixteen nanoseconds of delay is still too large for the purposes of this thesis. (Ref 21:399)

A big step towards miniaturization of microwave circuits such as time delay units can be realized through the use of stripline circuits. They do not exhibit good RF properties, but the shrinking of circuit sizes that is possible makes the loss of RF performance acceptable. The disadvantage of stripline arises in the fact that hybrid components are somewhat difficult to install. Figure 1 shows that stripline circuits require a dielectric layer and a ground plane both above and below the circuit plane. If one wants to include chip components in this structure, indentations in the dielectric (typically ceramic or teflon) must be made. As the

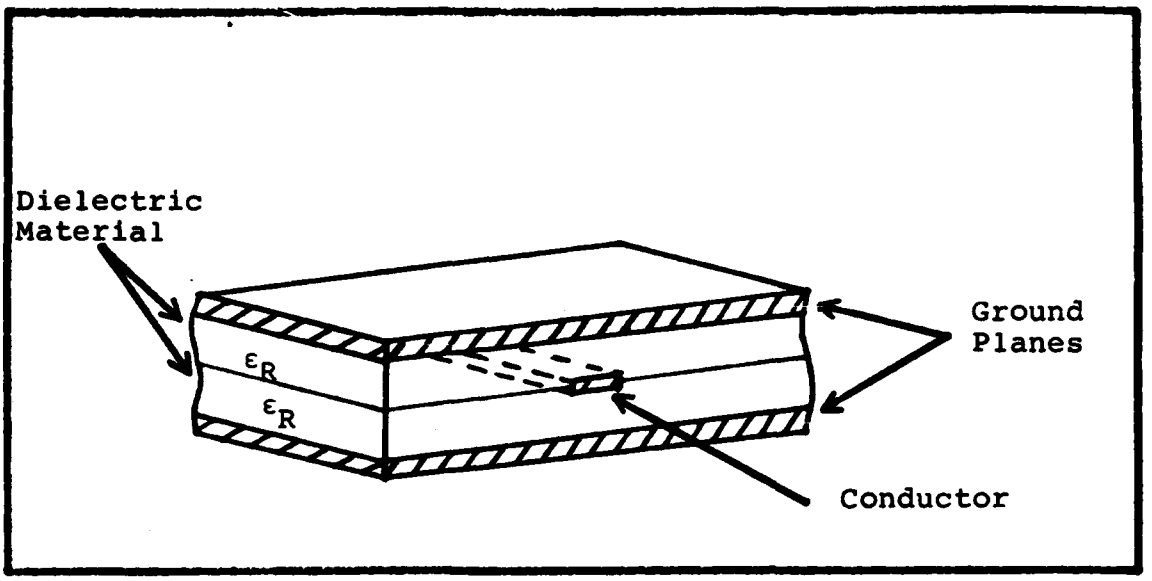


Figure 1. Example of Stripline Geometry.

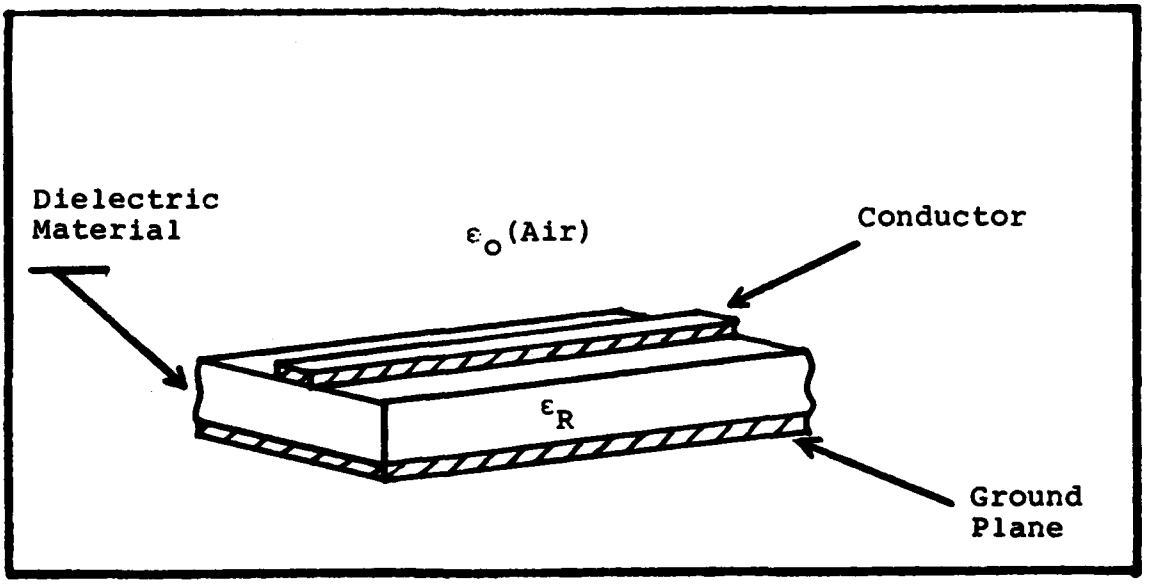


Figure 2. Simple Example of Microstrip Geometry

next paragraph will show, the fabrication of a stripline circuit is more rigorous than that of a microstrip circuit.

The fourth design alternative, microstrip, is very similar to stripline with respect to design and operation. The difference between the two can be seen in Figure 2. A microstrip circuit is built monolithically on a dielectric substrate, and its upper surface is left exposed to air. This openness makes attaching hybrid components simple. Again, Table I shows that the RF characteristics of microstrip are relatively poor with respect to those of waveguide and coaxial cable devices; however, the benefits of its ease of fabrication and excellent miniaturization potential make microstrip the prefered design technique for designing the circuit described in the specification section above.

For microstrip circuit fabrication, two substrates were available for this thesis: alumina ($Al_2 O_3$) ($\epsilon_R = 9.8$) and barium tetratitanate ($BaTi_4O_9$) ($\epsilon_R = 37.0$). Both are good microwave substrates up to 20 GHz, but their differences merit discussion. The most obvious difference is their relative dielectric constants. Since $BaTi_4O_9$ has a very high ϵ_R, transmission lines for a given amount of time delay will be shorter and smaller on it than on alumina. Therefore, $BaTi_4O_9$ is more desirable when compactness is sought.

The loss characteristics for the two materials are very similar, but the temperature coefficient for $BaTi_4O_9$ (-3.67 ppm/^{0}C) is much lower than that of alumina (+136 ppm/^{0}C). The exceptionally low magnitude of the temperature coefficient for $BaTi_4O_9$ translates into a very stable relative dielectric

constant for a large range of temperatures. Measurements have been performed over the range of -50°C to +100°C, and $BaTi_4O_9$ has proven to be the best known substrate material for temperature compensated microwave circuits. (Refs 21:19; 15:1629; 12:659)

The final aspect of comparison between the two materials is their cost. Alumina has been used for several decades and is in strong demand. Therefore, it is relatively inexpensive. This fact makes Al_2O_3 very good in a situation where many test circuits are to be made and experimented upon. Barium tetratitanate, however, has only been in use as a microwave material since the early 1970's. There is little experience with it, and it is relatively expensive and hard to obtain. So, due to cost and availability considerations, alumina was used as substrate material for the test circuits in this project and barium tetratitanate as the substrate for the final time delay circuit design.

Design Philosophies

Two specific design philosophies were explored; the first was a tapped line network, and the second was an N-bit switching network. This section presents the details of both and the reasons for selecting the second as the final design.

The tapped line network consists of one long transmission line with several intermediate taps, some are used as inputs and some as outputs. The amount of transmission line between the taps is chosen to produce a variety of delays. A specific

time delay is achieved by selecting an input and output port which have the needed amount of line between them to yield the desired delay. Figure 3 shows a simplified version of this described network. A practical version of this circuit would use switching diodes to allow the input of an RF signal into only one of the inputs and to pass this signal out only one ouput tap. This amount of time, , as inferred above, is directly proportional to the length of transmission line between theinput and output taps.

With the switching diode network only one input and one output will be conductive at any given time. Therefore, the input taps can be gathered together, and the output taps can also. Figure 4 shows the version of this configuration which was a candidate design for the final TDU.

The diodes in Figure 4 labeled with an "A" determine the RF path, and those labeled with a "B" aid in isolating the "switched out" paths from the one active path. The "B" diodes also help reduce ereflections of RF energy. This configuration yields a total of 32 possible path lengths, and in the case explored it gives a time delay of from one half to sixteen nanoseconds in one half nanosecond increments.

The advantage of a tapped delay line is that for delay timesin the lower portion of a given TDU's range, the RF signal will cross only a few diodes. Therefore, the insertion loss and reflections added by diodes will be relatively small for the shorter delays. This fact, though, leads to

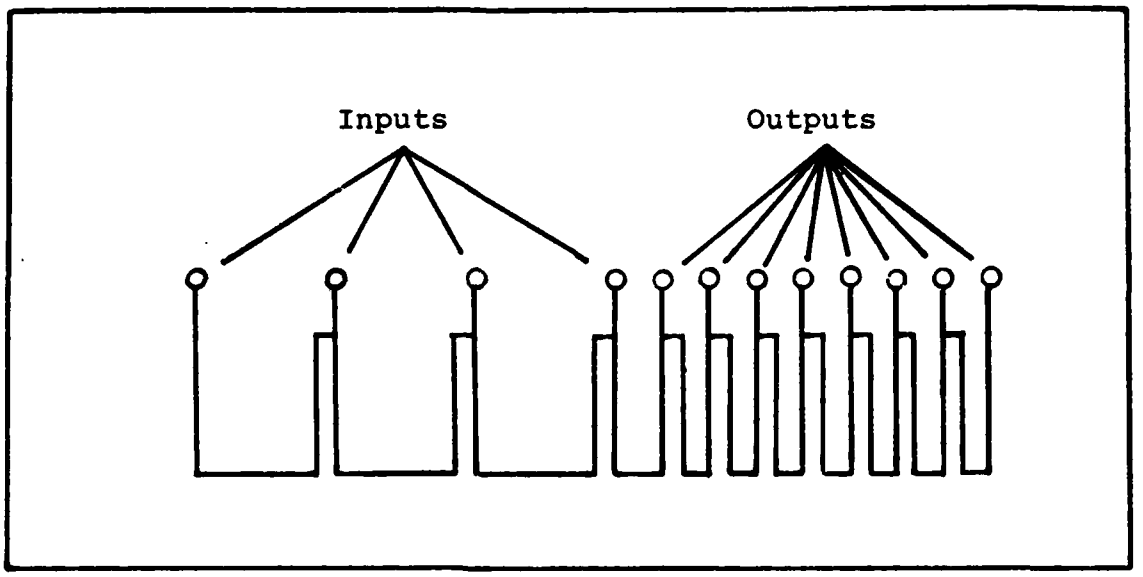


Figure 3. Simple Tapped Transmission Line Network.

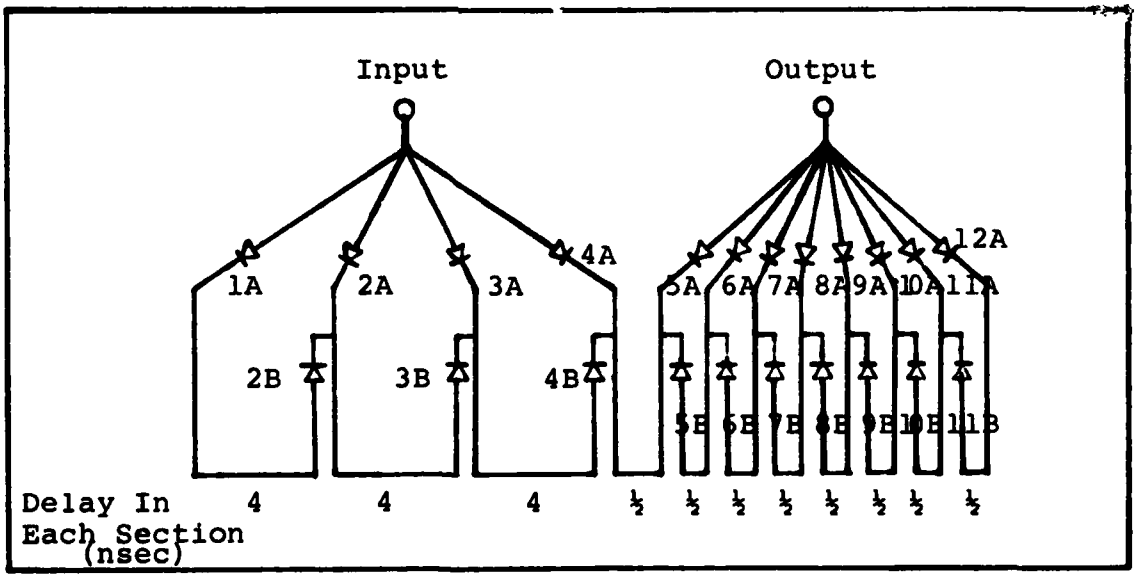


Figure 4. Layout of Tapped Line Design for ½ to 16 nsec TDU. (Bias Lines for diodes not shown)

the primary disadvantage of this configuration. The losses for various delay times will be widely different due to the varying number of diodes seen by the RF signal. Another disadvantage is all the transmission line junctions required for this design. A junction in a microwave circuit initiates reflections and losses, and tapped line networks will have many junctions. The example in Figure 4 even has one junction with eight lines feeding into it! This would be extremely lossy due to the variety of capacitances introduced by the many stubs connected to the junction. Because of the varying losses and the need for many junctions with the tapped line design, the N-bit delay line design was explored.

In an N-bit tapped delay line, each bit consists of two electrically parallel transmission line sections having different lengths and with switching diodes to select one path or the other, a bit can provide a choice between two amounts of time delay. A series combination of N bits can yield up to 2^N different delays. Therefore, a 5-bit configuration would be needed for the one half to sixteen nanosecond 32 step delay line discussed earlier. An example of a 5-bit delay line is in Figure 5.

For TDU applications this design has several advantages. First, the number of diodes in the active RF path is the same regardless of the path chosen. Therefore, losses introduced by diodes do not change when the time delay is varied. A second advantage of this configuration is that the overall design is simpler; all transmission line junctions are "T" junctions. The design can also be relatively easily expanded

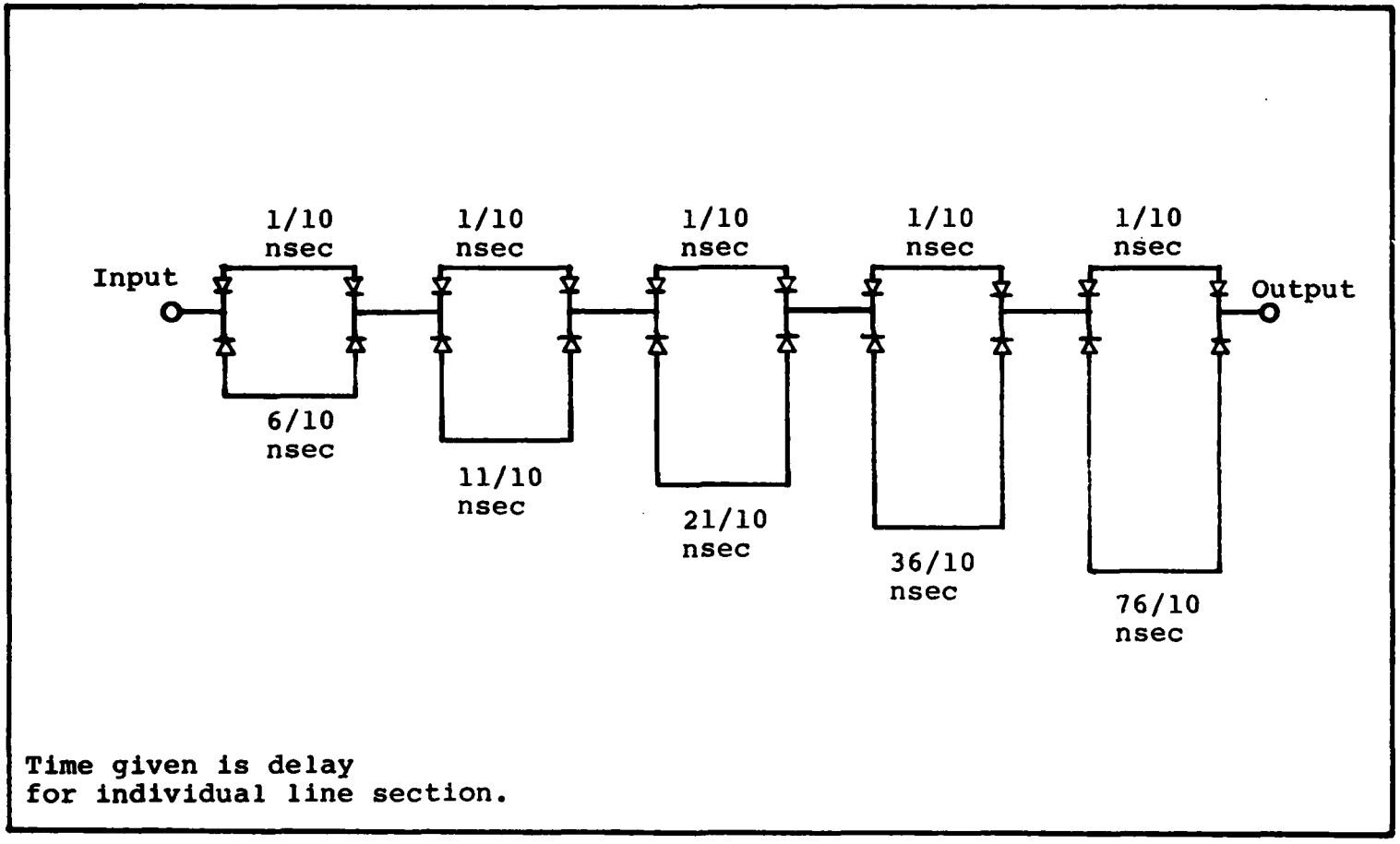


Figure 5. Schematic Diagram of a 5-bit TDU with a Delay Range of ½ to 16 nsec. (Bias lines for diodes not shown)

to broaden the delay range by adding more bits and making minor changes to the present ones. Details concerning a physical layout using this design are presented in Section III.

Microstrip Design Theory

Description of Technique. In 1949 the concept of the stripline microwave circuit was introduced. A few years later, microstrip design techniques were established. However, microstrip was not popular until the early 1970's when low loss dielectric materials were discovered. Since that time microstrip techniques have been applied to all types of microwave circuits. (Refs 23:67-68; 17:430)

A simple example of microstrip geometry is shown in Figure 6. In this figure h is the substrate thickness, w is the line width, t is the line thickness, and s is the spacing between lines.

Microstrip circuits are built monolithically on a dielectric material with hybrid components, if any, attached to the top of this circuit plane. As Figure 6, shows a microstrip line sees a relative dielectric constant of $\epsilon_R = 1$ (air) above it and $\epsilon_R > 1$ below it, resulting in an inhomogeneous dielectric medium. Figure 7 depicts the concentrating effect the high dielectric substrate has upon the field lines emitted from a microstrip line. To account for this dielectric discontinuity, an effective relative constant, ϵ_{RE}, is used in microstrip design equations. The value of ϵ_{RE} is dependent upon several things including w/h ratio

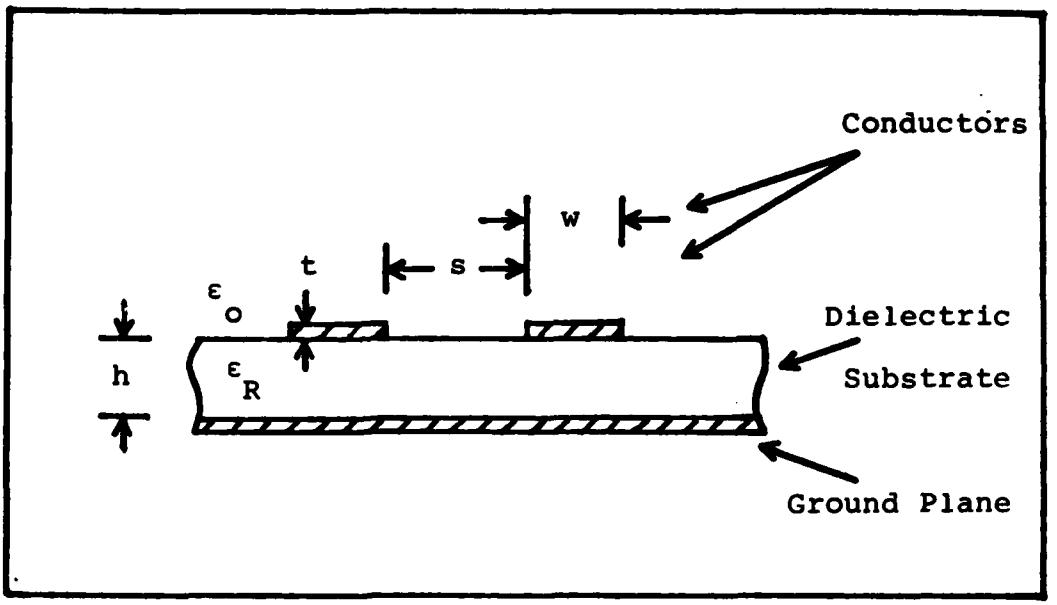


Figure 6. Detailed Example of Microstrip Geometry

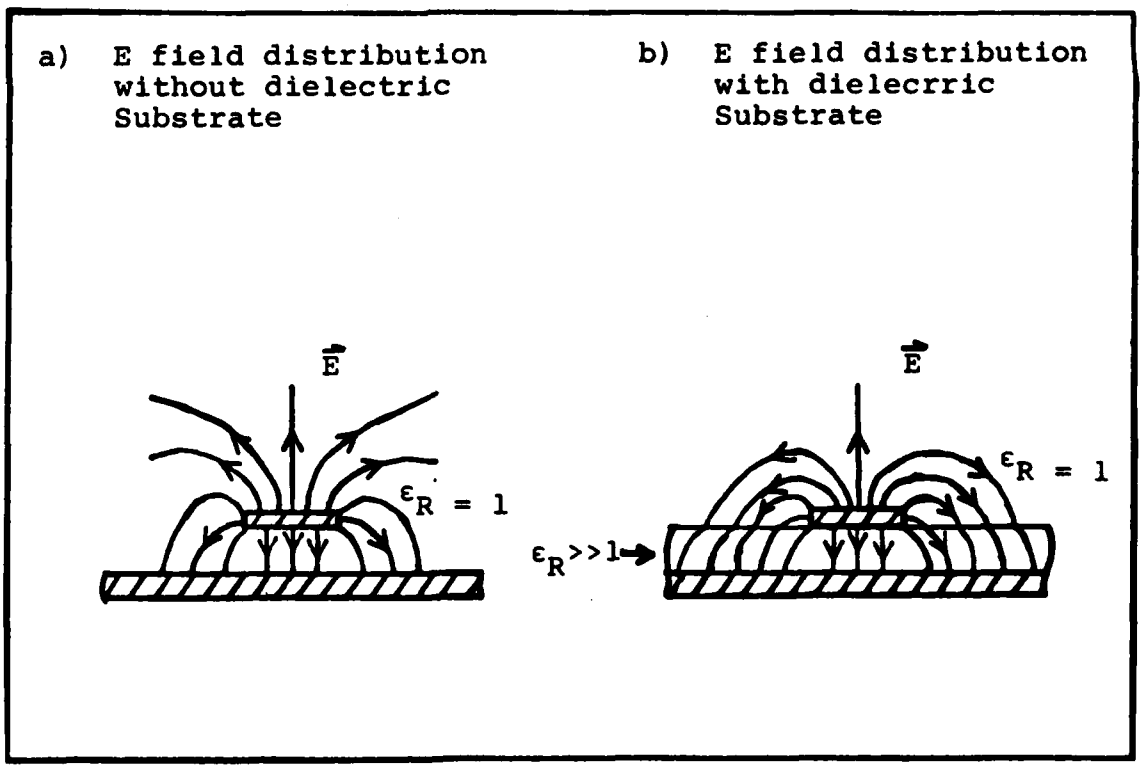


Figure 7. Microstrip Lines with their Electric Field Distributions. (Ref 5:43)

and frequency of circuit operation. The following section steps through the equations used to solve for ϵ_{RE} and other microstrip parameters. (Refs 7:3; 6:60-65)

Design Equations. For a microstrip time delay unit, the characterizing parameters are the microstrip line's width and length and the substrate's thickness. The line width to substrate thickness ratio determines the characteristic impedance (Z_o) of the line, and the physical length is proportional to the line's electrical length and therefore to its time delay. The parameters which must be established for a circuit design on a given substrate are: 1) the characteristic impedance of the transmission line, 2) the w/h ratio, and 3) the effective relative dielectric constant.

The first parameter that must be chosen is the characteristic impedance of the circuit. For this thesis, Z_o was set at 50 ohms to make the TDU compatible with its proposed environment. Next, the ϵ_R and h of the given substrate must be found. These values are applied to design equations to find the w/h ratio and ϵ_{RE}. Several approaches have been used in solving for these equations. Consequently, several versions of these equations exist, and each yields slightly different results. The equations derived by Gupta (Ref 6:60-65) were taken as the basis for this thesis. Gupta's approach to microstrip design was to theoretically solve the design equations and then experimentally prove their validty. For this thesis, the design parameters were found

using his equations and confirmed to within a few percent with several other sets of design equations. (Refs 16:53-55; 13:419-421)

The design equations used will be presented through the following example. The characteristics of the available barium tetratitanate substrate are: $\varepsilon_R = 37.0$ and $h = 2.0$ mm. Since Z_o has already been chosen as 50 ohms, the first parameter to be calculated is w/h. This ratio is given by the following equations.

For $A > 1.52$

$$w/h = 8 \exp(A)/(\exp(2A) - 2), \quad (1)$$

and for $A \leq 1.52$

$$w/h = (2/\pi)\{ B-1-\mathrm{Ln}(2B-1) + ((\varepsilon_R-1)/(2\varepsilon_R))\ (\mathrm{Ln}(B-1) + 0.39 - 0.61/\varepsilon_R)\ \}. \quad (2)$$

A and B are derived through

$$A = (Z_o/60)\ ((\varepsilon_R + 1)/2)^{\frac{1}{2}} + ((\varepsilon_R-1)/(\varepsilon_R + 1))\ (0.23 + 0.11/\varepsilon_R) \quad (3)$$

and

$$B = (60\ \pi^2)/(Z_o\ \varepsilon_R) \quad (4)$$

Knowing $Z_o = 50$ ohms and $\varepsilon_R = 37.0$, (3) can be solved to give a value of $A = 3.853$. Therefore, (1) would be used to yield $w/h = 0.16986$. Since $h = 2.0$ mm, $w = 0.340$ mm for a 50 ohm line.

Now to find ε_{RE}, the following equation would be used.

$$\varepsilon_{RE} = (\varepsilon_R + 1)/2 + ((\varepsilon_R-1)/2)(1 + 10\ h/w)^{-\frac{1}{2}} \quad (5)$$

For the ε_R and w/h given above, $\varepsilon_{RE} = 21.326$. This parameter

is important because it determines the physical length of a wavelength in a microstrip line.

$$\lambda_m = \lambda_o / \sqrt{\epsilon_{RE}} \qquad (6)$$

Here λ_o represents a wavelength in air, and $_m$ is a wavelength of the same frequency in a microstrip circuit. For example, at 3 GHz a wavelength in air is 100 mm, and in the microstrip line described above, the wavelength of a 3 GHz signal is 21.65 mm. Furthermore the velocity of an electrical signal through a microstrip line, V_m, is scaled down relative to the signal velocity through air, V_o, by the same factor.

$$V_m = V_o / \sqrt{\epsilon_{RE}} \qquad (7)$$

Therefore, for a TDU on a barium tetratitanate substrate, 64.96 mm (2.6 inches) of microstrip would represent one nanosecond as compared to approximately 210 mm (8.27 in.) of coaxial cable or waveguide. This example highlights the miniaturization feature of microstrip.

To facilitate discussion of actual microstrip designs in the following sections, the parameters of the available substrates are listed in Table II. Both the measured physical characteristics and the calculated design parameters are shown.

Fabrication Techniques.

The fabrication techniques used on the two types of substrates are very different. Since alumina is a very stable ceramic and capable of withstanding high temperatures, it can be processed using thick film techniques. Barium tetra-

Table II. Parameters of Available Dielectric Substrates

Parameters	Substrates	
	Alumina	Barium Tetratitenate
Substrate Size	3 in x 3 in x 0.025 in 76.2mm x 76.2mm x 0.635 mm	1.97 in x 1.97 in x 0.79 in 50 mm x 50 mm x 2 mm
h	0.025 in/0.635 mm	0.079 in/2 mm
ϵ_R	9.8	37.0
w/h	1.0	0.1699
w	0.025 in/0.635 mm	0.0134 in/0.340 mm
ϵ_{RE}	6.73	21.33
Length of 1 nsec section	4.55 in/115.67 mm	2.56 in/64.96 mm

titanate, however, should not be heated above 250°C. Therefore thin film processing techniques must be used on it. The following paragraphs describe these two fabrication procedures.

For thick film fabrication, once a design is complete it must be laid out on either vellum or rubylith at any desirable scale. The two test circuit layouts for this

thesis were done at a 4x scale on vellum. Next the circuit design is photographically reduced to a 1x scale and placed on a mylar film. This picture of the circuit is used as a mask for a fine stainless steel screen coated with photographic emulsion. After exposure through the mask and development of the emulsion, a negative copy of the circuit is left on the screen; the areas where thick film metal is wanted for the circuit are clear, and the rest of the screen is blocked by emulsion. Then the screen is placed directly on the substrate, and conductive ink is forced through the open areas of the screen leaving a printed version of the circuit on the substrate. After the substrate is fired at a high temperature (800 - 1000°C depending on the thick film ink used - 800°C in this case), hybrid components such as diodes are mounted on it, and the circuit is ready for use.

As with thick film, the first step for thin film fabrication is to lay out the design on vellum or rubylith. The final circuit design for this thesis was placed on rubylith at 20x. Next, the design must be reduced to a 1x scale and put on a glass plate. This plate is used later as a photolithographic mask. Then through evaporation, the substrate is coated with 150 angstroms of chromium and 1000 to 2000 angstroms of gold. The chromium is needed for adhesion, and the gold acts as an electrode for gold plating. After the metal, a layer of thick photo resist (0.001 in. for this thesis) is applied, and the mask made earlier is used to define the circuit pattern in the resist. After the photo

resist is developed, windows are left in the resist layer where metal is desired. Then 5 microns of gold are deposited in these windows by gold plating, and the remaining resist is removed. The evaporated chromium and gold are then chemically etched, and only the circuit pattern is left. (Refs 15:1628; 12:655) Finally, the hybrid components may be attached, and the circuit is completed. The process steps for thin film and thick film fabrication are summarized in Figure 8. (Ref 23:30-48)

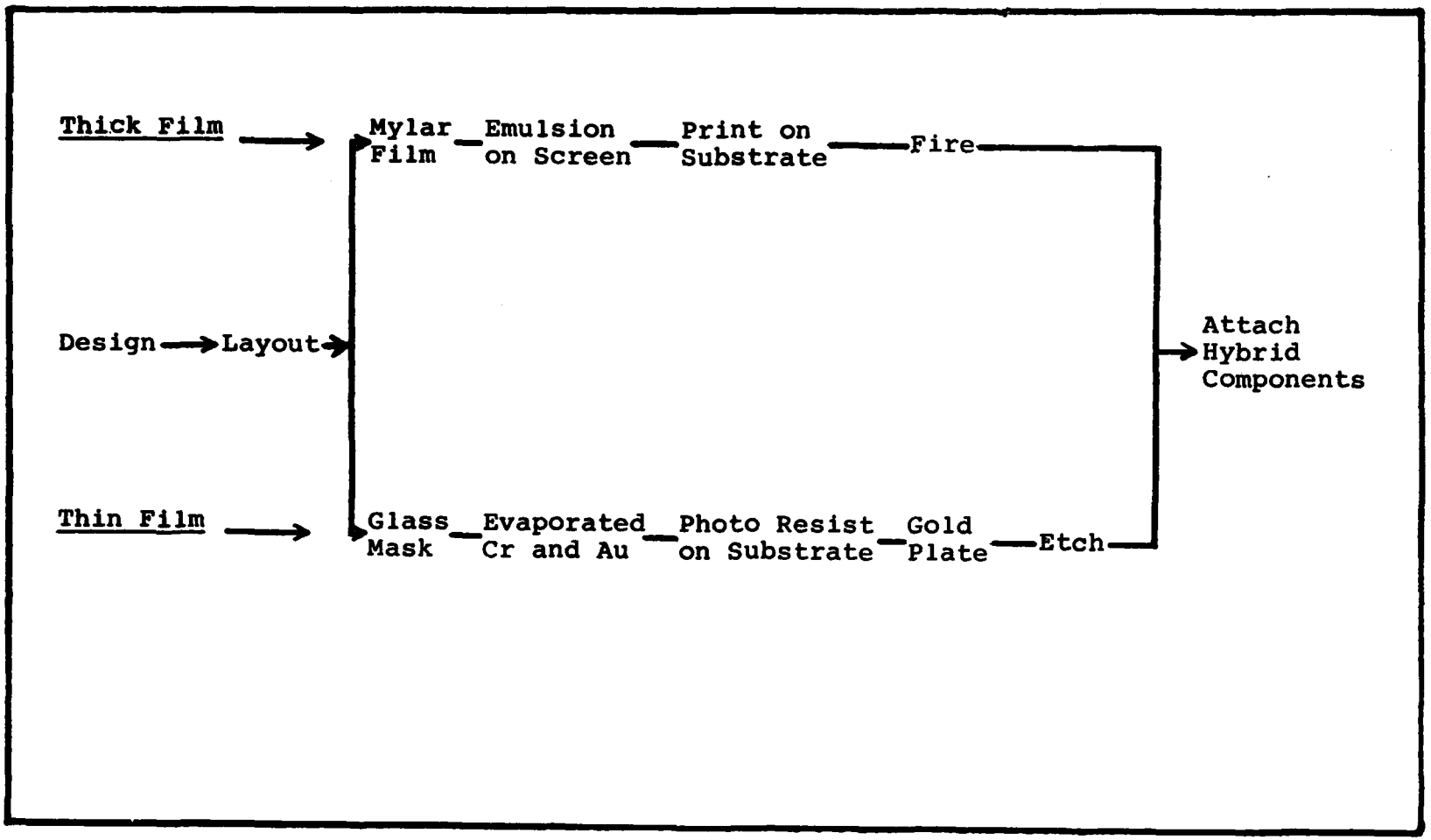


Figure 8. Summary of Fabrication Steps For Thick Film and Thin Film Processing

III. Time Delay Unit Designs and Test Circuits

Two different design philosophies for this time delay unit were explored - a tapped transmission line and an N-bit network. In this section, the details of each design type are given. Then the test circuit used to determine the feasibility of each design type is discussed along with the results of the tests performed on the circuit. The tapped transmission line design will be presented first, followed by the N-bit network design.

Tapped Transmission Line Design

Design. The basic shape of a TDU built using the tapped transmission line design is shown in Figure 4. The original design specification for this TDU was for a delay range of ½ to 16 nanoseconds in ½ nanosecond increments. So the total length of the transmission line must be equivalent to 16 nanoseconds, and the shortest section which could be connected to the input and output taps has to equal ½ nanoseconds. To achieve this delay variation the transmission line could be divided into 32 one half nanosecond sections in a cascade arrangement. This configuration, however, would produce a very lossy meander line due to all the switching diodes needed to control the RF signal path. Therefore, the line was divided into four groups: three sections of 4 nsec delay each and one section of eight ½ nsec steps. This arrangement allows for a delay of up to 16 nsec in ½ nsec steps through the selection of 0,1,2, or 3 of the 4 nsec groups plus 1 to 8 of the ½ nsec

steps. Figure 9 shows the physical layout of this configuration without the control lines for the diodes.

As Figure 9 shows, the input line to the TDU feeds four taps. Three of the taps feed 4 nsec line sections, and the fourth feeds the group of ½ nsec steps. The output line takes the RF signal from one of the eight ½ nsec sections. The path selection is controlled by turning on (forward biasing) certain diodes and turning off (reverse biasing) the rest of them. For the diode numbering scheme shown, only two "A" diodes would be on at a given time, one from "1A" through "4A" and the other from "5A" through "12A". For this configuration, the "A" diodes are the primary steering diodes. The "B" diodes isolate the switched out paths from the active path and reduce reflections. The 32 different delays allowed by this TDU make the biasing scheme moderately complex. However, one will note that which ever direction an "A" diode is biased, its corresponding "B" diode will be oppositely biased. For example, if "4A" and "5A" are forward biased, "4B" and "5B" would be reverse biased. This situation yields a ½ nsec delay.

A final aspect of this design is isolation of the diode biasing voltages. The dc voltage for biasing one diode must not inadvertently interact with other diodes. This problem is easily solved by placing dc blocking capacitors between the individual diode subnetworks. In all, this design would require 24 capacitors and 22 diodes.

Layout of Test Circuit I. The purpose of this first test circuit was to determine the feasibility of the tapped

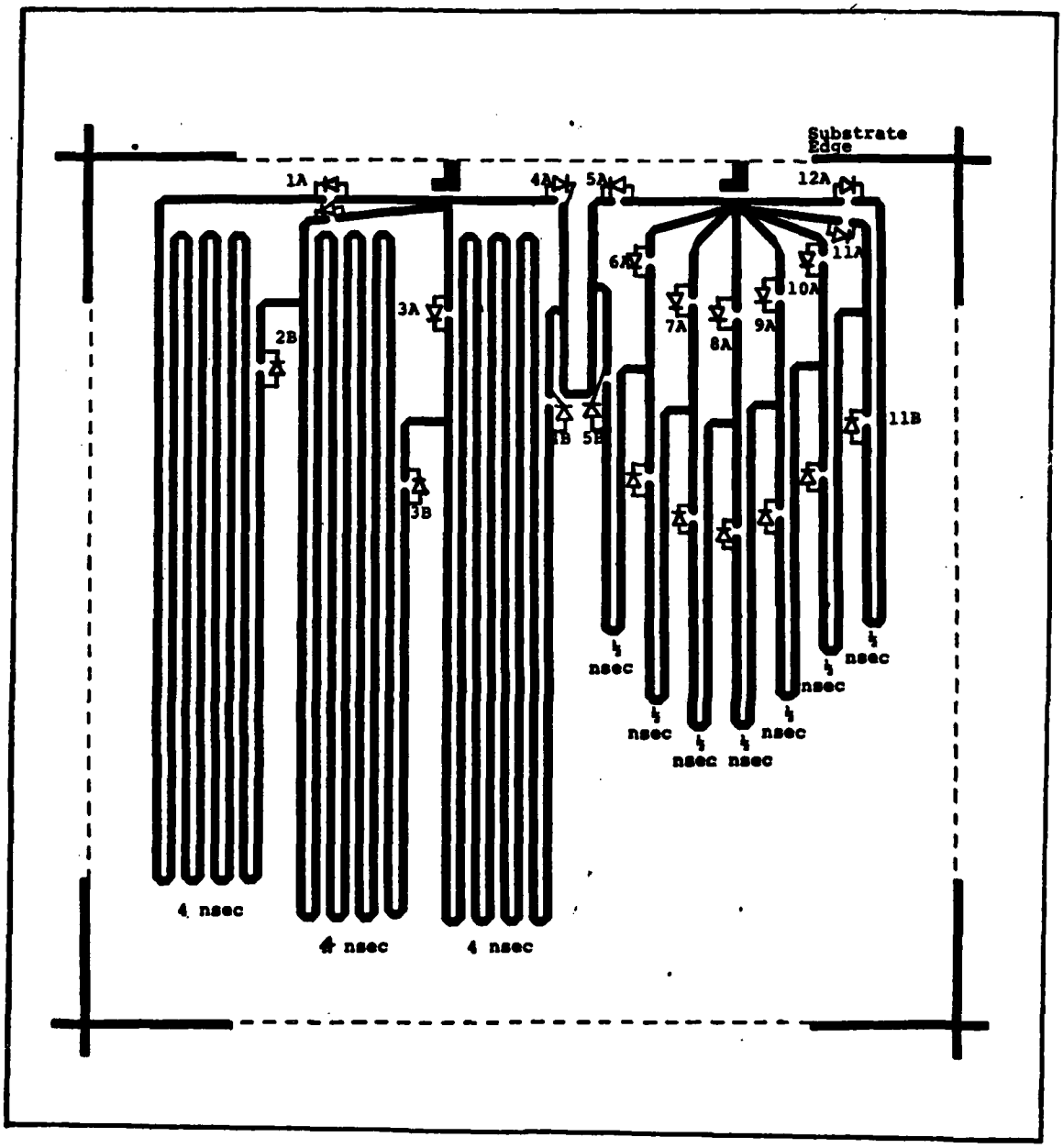


Figure 9. Physical Layout of ½ to 16 nsec Tapped Transmission Line TDU.

transmission line design. It was constructed on a 3 inch by 3 inch alumina substrate using the thick film processing technique explained in Section II and was designed to fit in the microwave test fixture shown in Appendix B. This subsection explains the details of the test circuit.

The circuit can be divided into three sections: 1) a 4 nsec transmission line, 2) a ½ and 1 nsec transmission line group, and 3) bond wire inductor pads. Figure 10 shows this circuit with these divisions marked. Sections 1 and 2 are geometrics transposed exactly as they would appear on the full TDU of this design type, and section 3 consists of geometrics proposed as inductors for the TDU.

The first section, the 4 nsec line, was taken from the TDU design to show the effects of a small w/h and s/h ratio. Since a 4 nsec length of transmission line is much longer than the length of the substrate, the line must meander back and forth several times. The small surface area of the substrate necessitates limiting the spacing between parallel runs of line to 0.025 inches. Since "h" for the alumina substrates is 0.025 inches, the s/h ratio is 1. This ratio is the largest allowable for this TDU design on this substrate. Furthermore, the length over which these lines run parallel to each other is about 1.5 λ_m (at 3 GHz). This combination of small s/h and long parallel line length predicts a significant amount of coupling between parallel lines. Unfortunately, this coupling would degrade the circuit's VSWR. (Ref 17:54)

The ½ and 1 nsec group of transmission line was chosen to demonstrate the effects of transmission line junctions on the

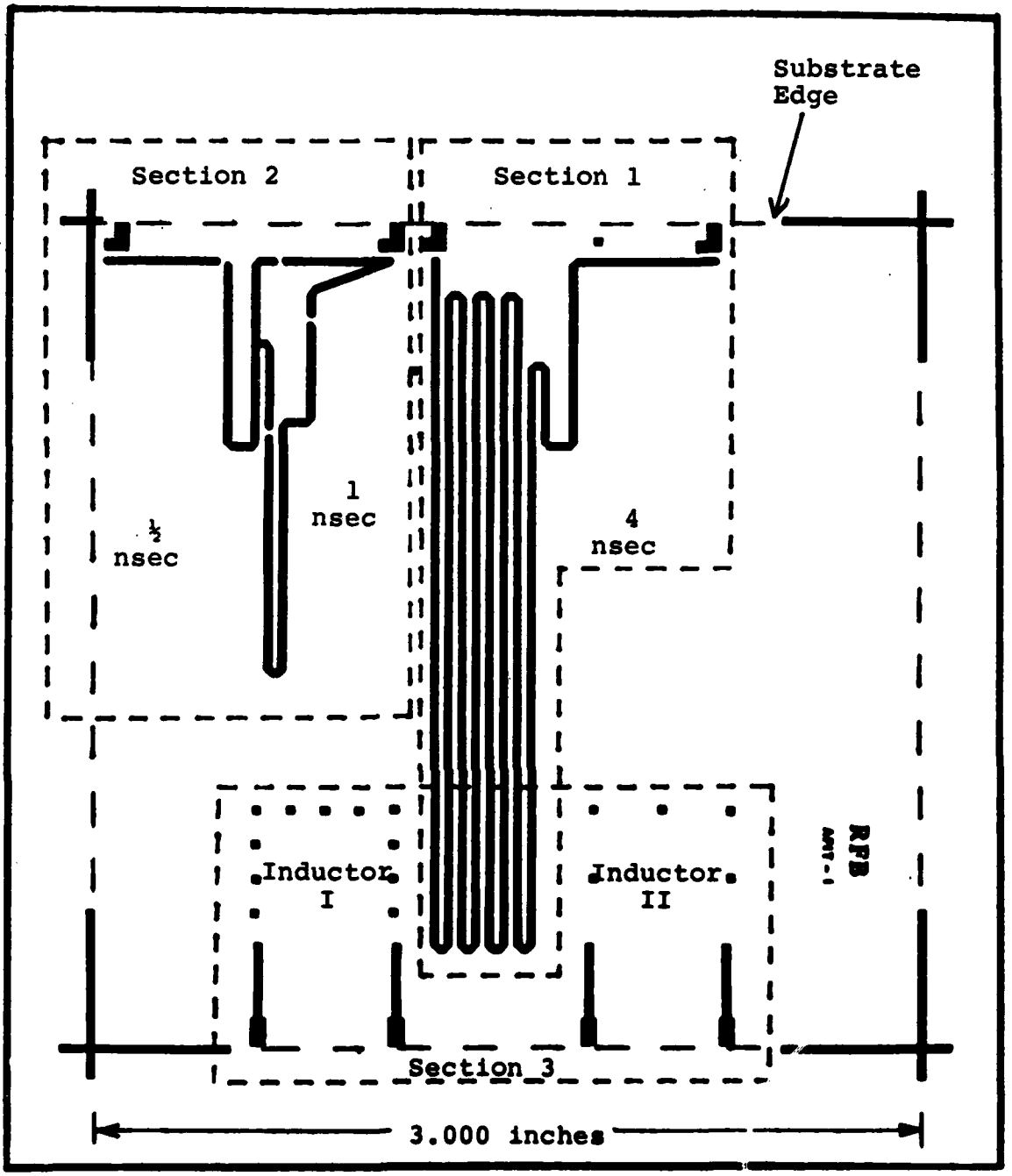


Figure 10. Physical Layout of Test Circuit I.

RF characteristics of the circuit. This section emulates the ½ nsec and 1 nsec delay increments on the full TDU design of Figure 9. Breaks in the transmission line were left at the points where diodes would be attached. The diodes which would be used for selecting paths in this TDU are chip type PIN diodes. They are attached by connecting one terminal (the base of the chip) with conductive epoxy to the transmission line on one side of a break. The other terminal (the top of the chip) would then be connected with bond wire to the line on the other side of the break. In section 1 of the test circuit these breaks were selectively jumpered with bond wire to allow for either a ½ or 1 nsec length of line between the input and output taps.

The final feature of the test circuit is the bond wire inductor pads. These bonding pads were designed to determine if the inherent inductance in 1 mil bond wire is sufficient to make the bond wire device act as an RF choke. The following equation predicts the inductance of a round wire of length L and diameter d, both dimensions in mils. (Ref 23:151)

$$L_W(nH) = 5.08 \times 10^{-3} \, L \, (\ln(L/d) + 0.386) \qquad (8)$$

The two geometries placed on the test circuit are: 1) 0.025 in. by 0.025 in. square pads in a 1.5 in. long line with 0.1 in. spacing between the pads and 2) pads of the same size in a 1.5 in. line with 0.25 in. spacing. Using (8) gives a value of about 60 nH for the 1.5 in. long bond wire; this translates to about j180 ohms at 3 GHz. The following subsection lists the test results for all the test circuit geometries shown above.

Experimental Results. Listed here are the test results for Test Circuit I. The various circuit parameters were found in accordance with the procedures detailed in Appendix A. The frequency range over which these measurements were taken is 2.5 GHz to 3.5 GHz. Following the listing is a discussion of the test results.

Section 1 (2.5 to 3.5 GHz)
4 nsec transmission line

Insertion Loss	from 2 to 7 db (Figure 11a)
Delay	from 2.9 to 5.3 nsec (Figure 11b)
VSWR	maximum of 20 (Figure 11c)

Section 2 (2.5 to 3.5 GHz)
½ nsec transmission line

Insertion Loss	from 5 to 11.5 db (Figure 12a)
Delay	from 0.49 to 0.87 nsec (Figure 12b)
VSWR	maximum of 40 (Figure 12c)

1 nsec transmission line

Insertion Loss	from 10 to 22 db (Figure 13a)
Delay	from 0.6 to 1.6 nsec (Figure 13b)
VSWR	maximum of 100 (Figure 13c)

Section 3 (2.5 to 3.5 GHz)

Inductor I (0.10 in. spacing)
Reactance - highly sensitive to frequency (Figure 14a)

Inductor II (0.25 in. spacing)
Reactance - highly sensitive to frequency (Figure 14b)

Overall, these results show the tapped transmission line design to be a relatively impractical design due to high loss and high VSWR. One will note that the insertion loss is much higher for the ½ nsec and 1 nsec sections of line than for the 4 nsec section. This increase is caused by the larger number of transmission line breaks for diodes in these sections than in the 4 nsec section. These breaks also aide in raising the

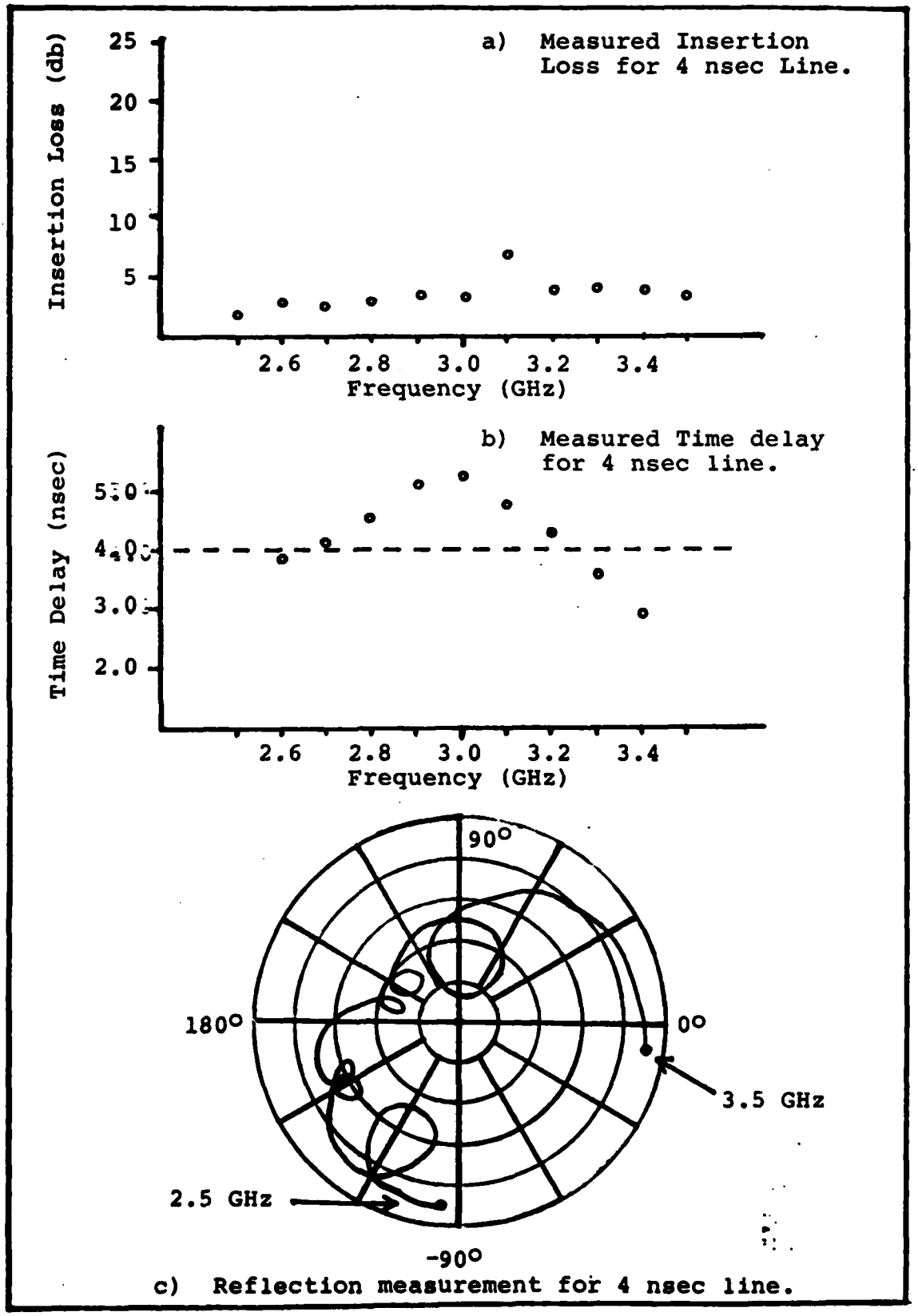


Figure 11. Plots of Measured Parameters Versus Frequency for 4 nsec Line Section on Test Circuit I.

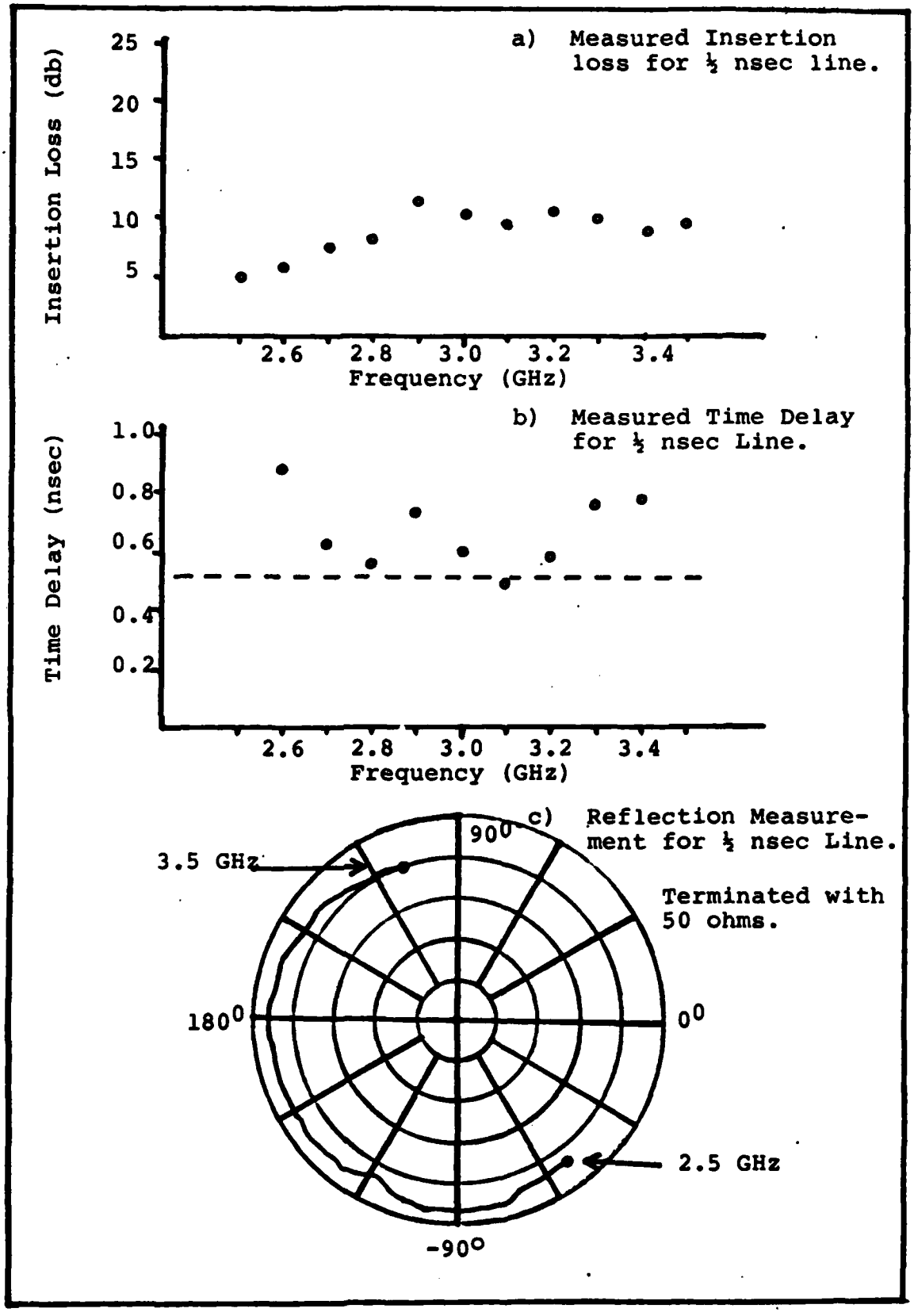


Figure 12. Plots of Measured Parameters Versus Frequency for ½ nsec Line Section on Test Circuit I.

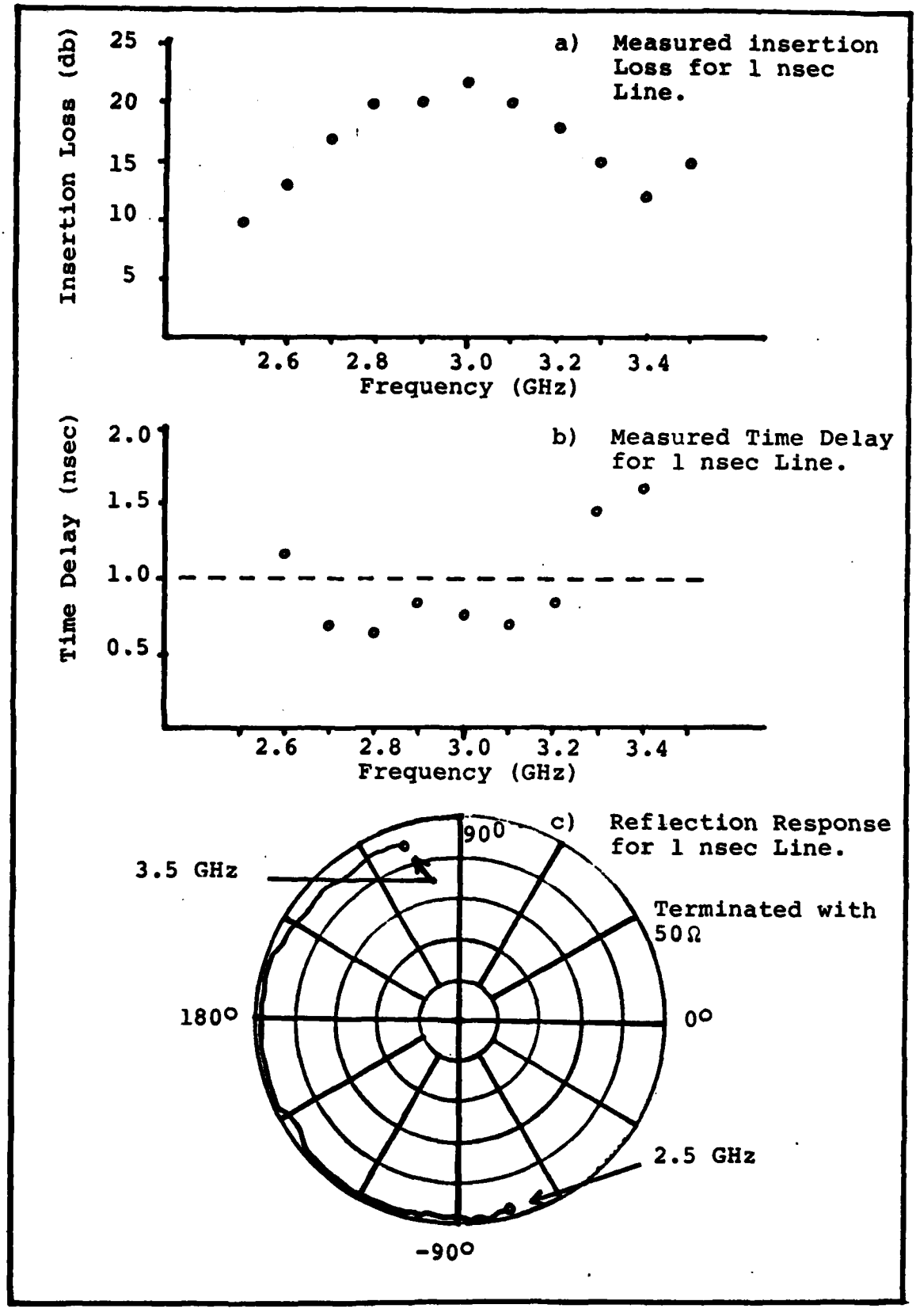
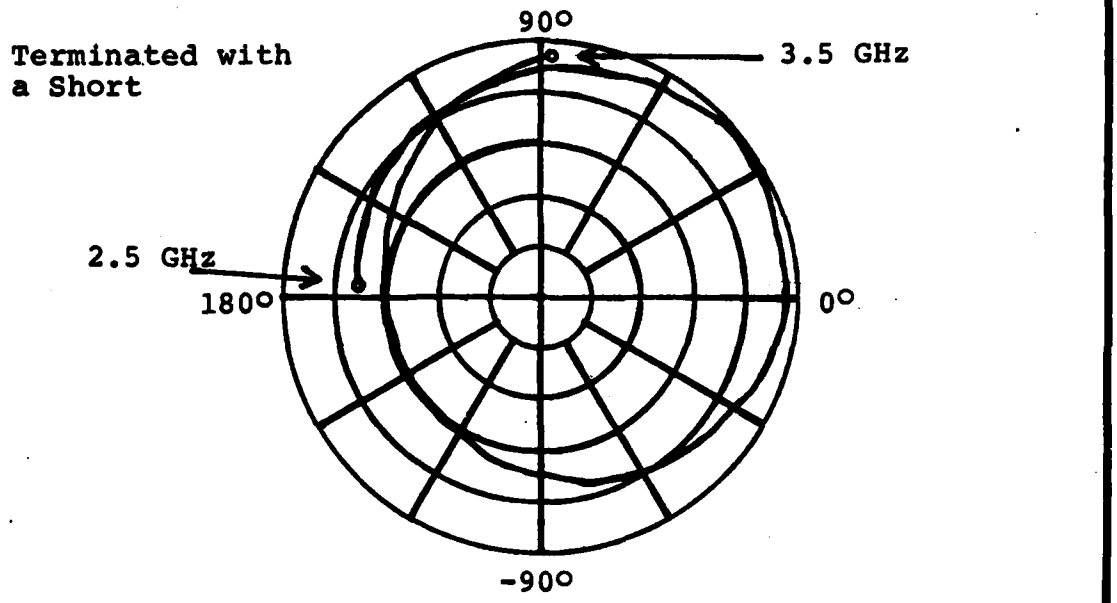
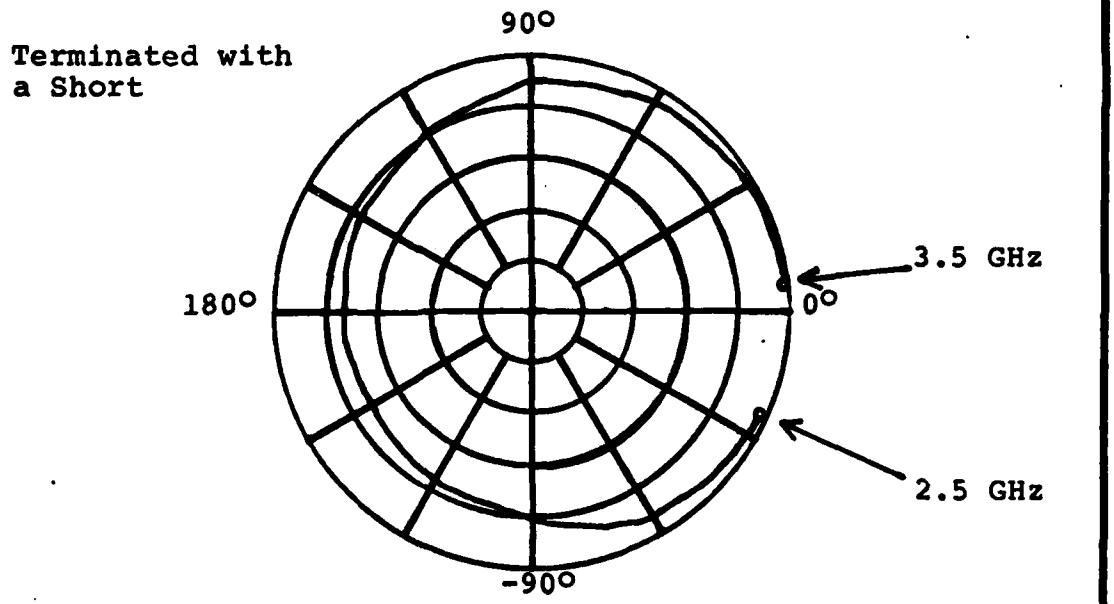


Figure 13. Plots of Measured Parameters Versus Frequency for 1 nsec Line Section on Test Circuit I.



a) Reflection Response for Inductor I.



b) Reflection Response for Inductor II.

Figure 14. Plots of Reflectometer Output for Inductors I and II on Test Circuit I.

VSWR of the two smaller sections. The high VSWR of the 4 nsec section is caused in part by the two line breaks for diodes, but primarily it is brought about by the side coupling of the relatively long parallel lines.

Another effect of this coupling is the widely varying time delay in all three transmission line sections. As would be expected, the 1 nsec and 4 nsec sections, which both have runs of parallel lines with an s/h = 1 spacing, show a larger variation in time delay over the 2.5 to 3.5 GHz.range than the ½ nsec section. The ½ nsec line which does not have any parallel line sections that run close together still has a delay variation of about 75% over the 1 GHz spread. This nonuniformity is caused by a combination of line breaks and line junctions.

The performance of the two test inductors was far from expected. With 1 mil bonding wire connecting the bonding pads in a loop from input to output tap, the impedance of these "transmission line" inductors proved to be highly sensitive to frequency. This sensitivity can be explained through a lumped element model of a transmission line as shown in Figure 15. (Ref 22:538) The L term is the inherent inductance in the line (bond wire in this case), and C is the shunt capacitance. The major source of shunt capacitance in these bond wire inductors is the intermediate bonding pads used to position the 1.5 inch length of wire. The aim of the design for Inductors I and II was to have the inductive reactance (x_L) much higher than the microstrip characteristic impedance (z_o) and to have capacitive reactance high enough to not effect the transmission line's inductance ($X_C \rightarrow \infty$). An acceptable

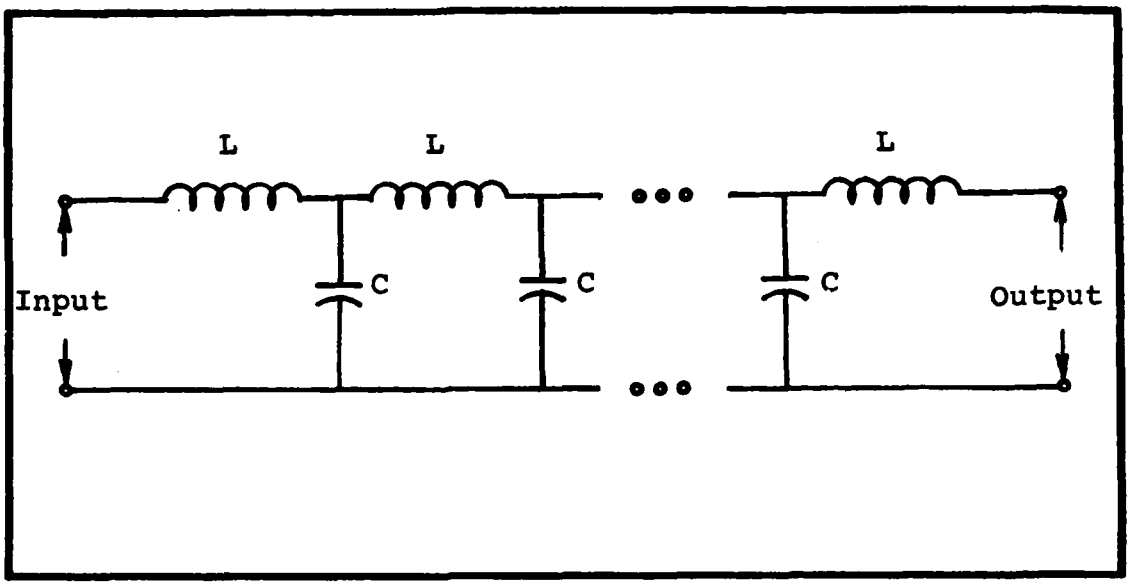


Figure 15. Lumped Element Model of A Transmission Line. (Ref 22:538)

value of inductive reactance is j250 ohms ($X_L \geq 5Z_o$). Assuming very small resistance, this reactance converts to an angle between 0 and 25 degrees on a network analyzer's polar display.

Inductors I and II, as their reflection response plots show, have an impedance that is a rather complex function of frequency. Apparently, the inductors' shunt capacitance is not very large ($X_C \not\to \infty$) with respect to its inductance. Thus the bonding pads appear to be degrading performance.

Another source of capacitance, although a small one, is the wire's inherent shunt capacitance. This is usually considered negligible, but it could be significant for this type of bond wire and this inductor design.

Several conclusions were reached with this data. First, a reduction in the number of junctions and breaks in the transmission would be needed in order to reduce losses. For this

reason the N-Bit design was investigated. Next, the relative spacing between parallel lines must be increase do coupling will be reduced. Finally, a different inductor geometry must be found. Two routes were explored: 1) characterize the bond wire impedance (without bonding pads) and 2) investigate would wire inductors. The second test circuit incorporates all of these recommended changes.

N-Bit Design

Design. After getting relatively poor results with the tapped transmission line design, the N-bit TDU was investigated. As will be shown below, this basic design yielded much better test results. The design used as the second test circuit is that of a 5-bit time delay line. Using five bits allows 32 different states or delays, thus the ½ to 16 nsec range can be covered in ½ nsec steps.

The concept of a bit switch, as discussed in Section II, is a simple one. The switch consists of two transmission line sections with one longer than the other. When the switch is in state "0", one section, the shorter one for this example, is connected between the input and output lines. The longer line is electrically disjointed from the RF path. In state "1", the opposite is true. The longer line section is switched into the RF path, and the shorter one is switched out. Thus, like a binary bit, a bit switch has only two states.

The switching in a bit switch is performed by diodes placed on the ends of each line section and is controlled by dc bias voltages. Figure 16 demonstrates the operation of a

bit switch. The inductors shown keep the RF energy out of the dc control system, and the capacitors block the dc from the RF system. One will note that signal "$\bar{A}$" is simply the logical inverse of "A". For a 5-bit TDU ten control signals are needed - five independent signals and the inverse of each one of these.

As with tbinary bits, a string of N-bit switches yields 2^N states. The TDU explored here is a simple 5-bit switching scheme with its 32 states. Figure 5 depicts this circuit, although it is over simplified. For the actual design, the delay introduced by the line sections between bits and those on the outside of the first and last bits must be taken into account. The delay lengths considered for this design are shown in Figure 17.

For this design the insertion loss is expected to be lower than for a comparable tapped transmission line design because of the simpler, cleaner design. All transmission line junctions for bit switches are simple "T" junctions which exhibit better microwave characteristics than the junctions at the input and output taps of the tapped line circuit in Figure 9. For this same reason, the VSWR of a 5-bit TDU can be expected to be much lower than for the other design. These characteristics, insertion loss and VSWR, are examined through tests on test circuit II.

Layout of Test Circuit II. The sequence of events leading to this second test circuit was very similar to that of the first one. A full TDU design was drawn up, parts of it

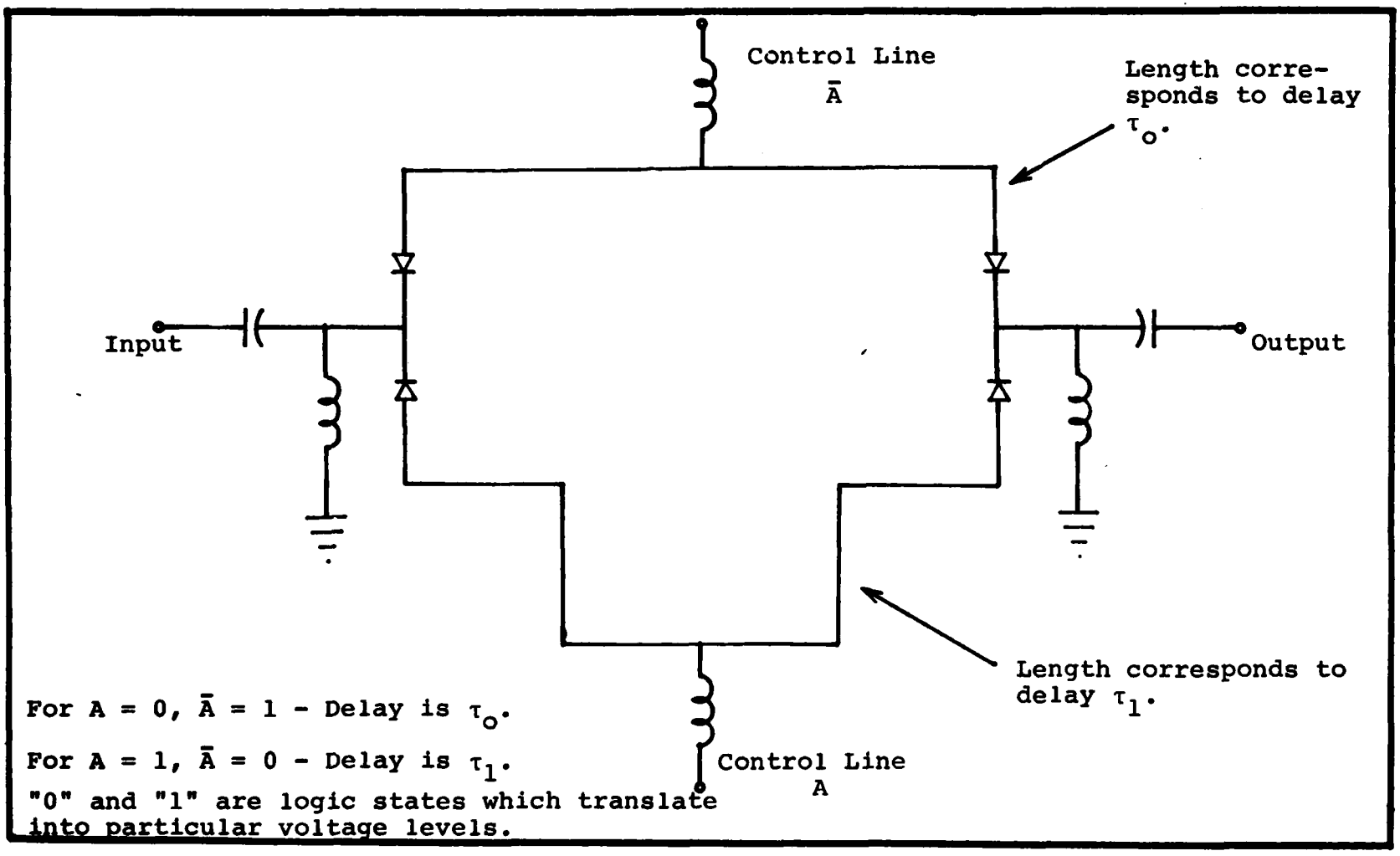


Figure 16. Circuit Model of a Bit Switch.

were chosen to be placed on the test circuit, and a composite layout was made. As with the first circuit, the layout was dimensioned for a 3 inch by 3 inch alumina substrate and designed to fit in the microwave test fixture shown in Appendix B. The circuit was fabricated with thick film processing steps.

The purpose of this test circuit was to prove or disprove the conjectures already stated about the 5-bit TDU design. Figure 18 shows the layout of Test Circuit II. To facilitate discussion of the circuit, it is split into three sections: 1) a ½ nsec header, 2) a header with four bits attached, and 3) three sets of inductor test pads.

Referring back to the circuit shown in Figure 17, the physical geometry of these bits can be easily arranged to yield a structure such as the one shown in Section 2 of this test circuit. For this configuration the short segment of each bit is placed in a straight line with the line sections between the bits. Thus the minimum delay path through the TDU is physically a straight path. This path can be viewed as a header onto which the five bits are attached. Section 1 of the test circuit embodies precisely this type of transmission line header. Its length corresponds to a calculated value of ½ nsec, and the squares placed on the line near the input and output are pads for mounting chip capacitors for dc blocking. For testing purposes capacitors were not mounted to the circuit, but since they would appear on the final design, the pads were included here.

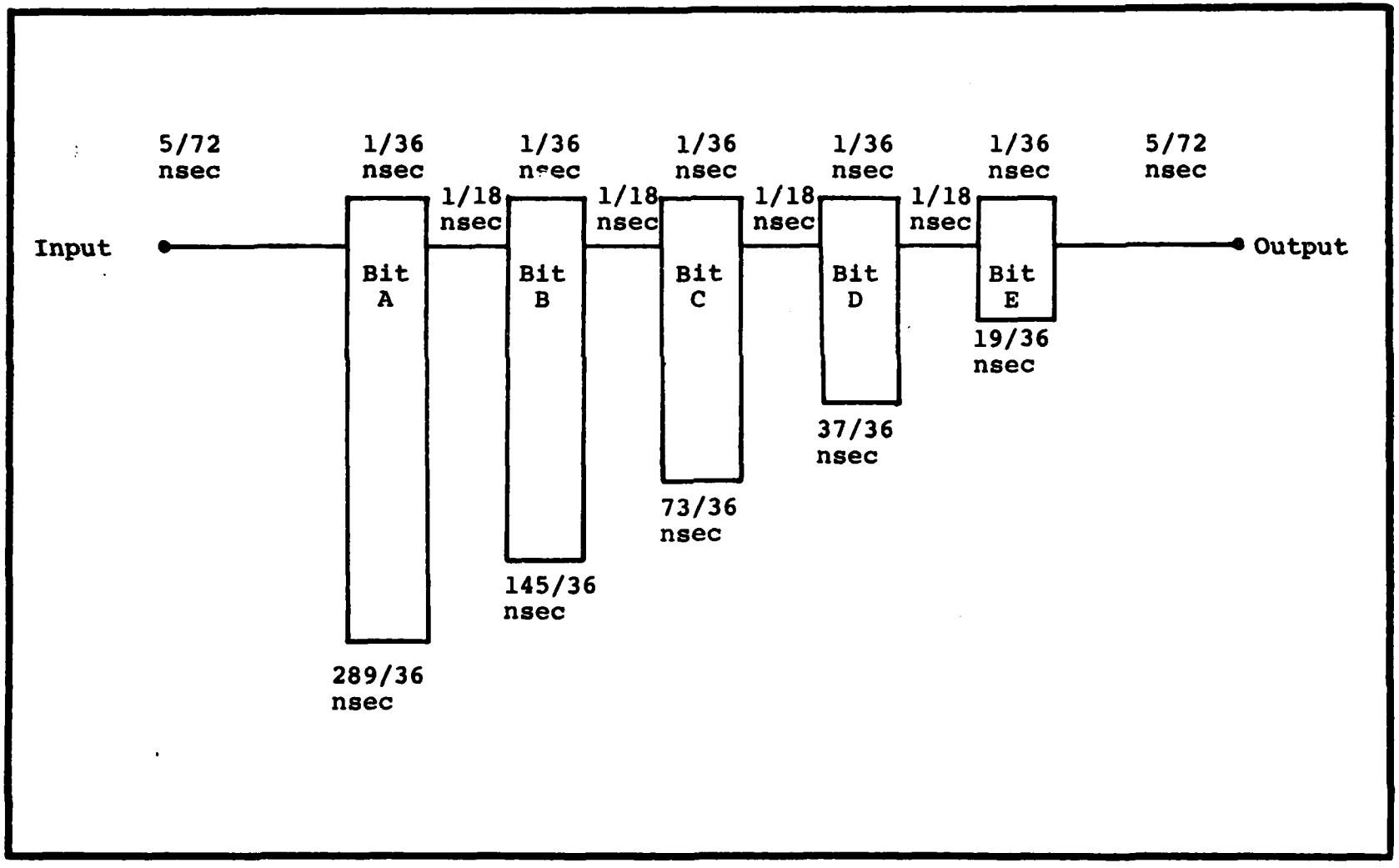


Figure 17. Schematic Diagram of a 5-Bit Variable TDU With a Time Delay Range of ½ to 16 nsec.

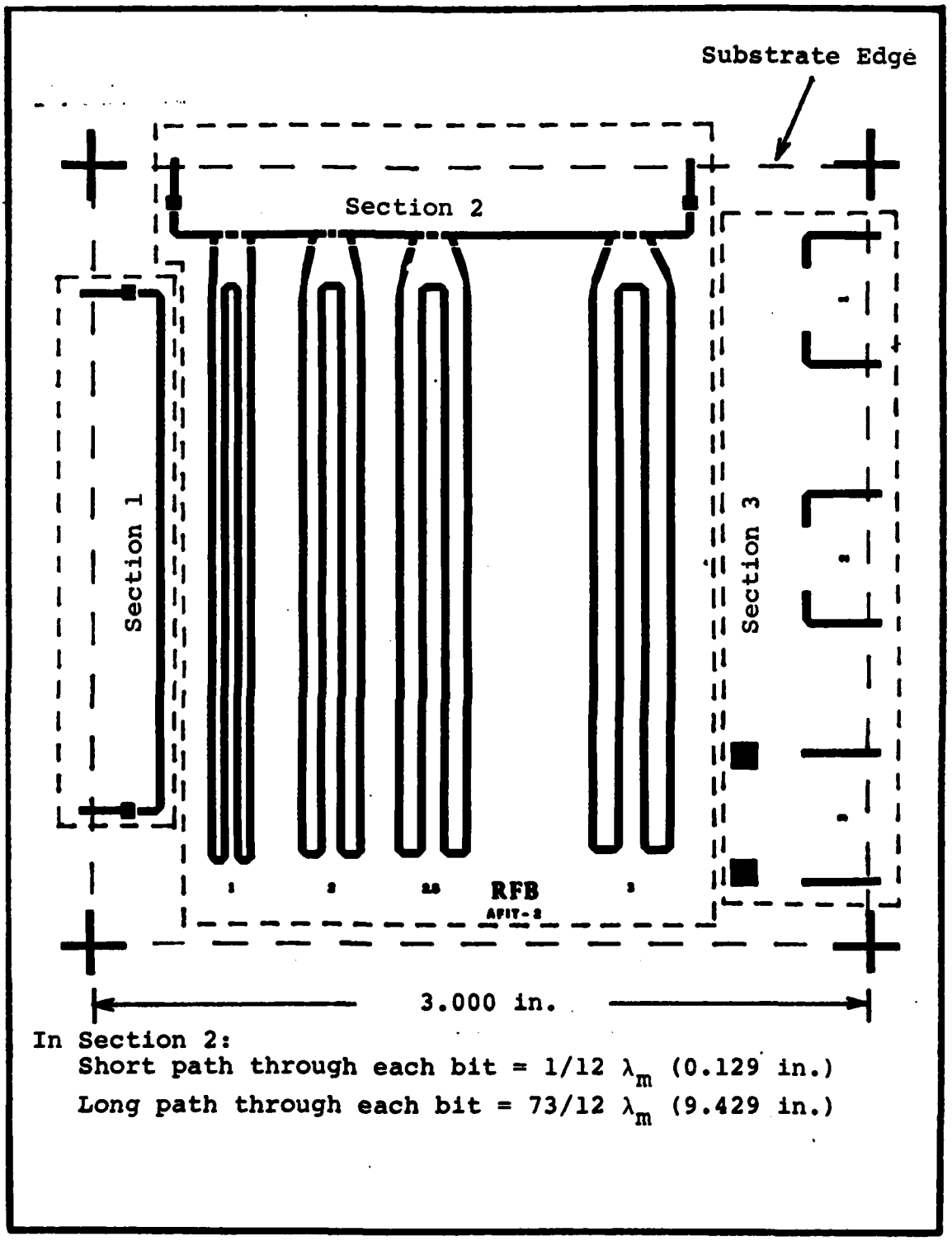


Figure 18. Physical Layout of Test Circuit II.

As mentioned above, Section 2 depicts a collection of bits - 4 bits for thise case. Since the relationship between the s/h ratio and coupling was identified on Test Circuit I, the bits in Section 2 were designed to examine this relationship. The number labeling each bit (located at the bottom of the bit) represents the s/h ratio for the meandering line portion of that bit. To keep all other variables the same for each bit, the short path through each bit is the same length, and the long path in each is equal in length. The lengths chosen are those calculated to yield a 2.5 nsec delay for the selection of the long path in any one bit plus the short paths in the other three. Therefore, these bits resemble Bit C in Figure 17. The header length is the same as in Section 1, ½ nsec, so one will note that the long path in each bit is 2 nsec longer than the short path.

The breaks in the transmission line are the points where chip diodes would be located. For the purposes of this test circuit, though, bond wire jumpers were used to select the desired path through each bit.

The third portion of the test circuit, the inductor test pads, was needed for finding a feasible RF choke for the final TDU design. The lines labeled 1 and 2 were used for testing several different lumped inductors including three Piconics brand RF chokes and two hand would chokes. The third set of pads is designed to examine the parameters of just the bond wire. The two printed leads shown in Section 3 are 50 ohm lines with a 0.5 inch spacing between them. By connecting a bond

wire between the lines, the impedance characteristics of just the bond wire for the desired frequency range can be viewed. The test results for Test Circuit II are given in the next section.

Experimental Results. The test results for Test Circuit II are shown below. The results were attained through the test procedures defined in Appendix A. The significance of the results is reviewed following the listing.

Section 1 (2.5 to 3.5 GHz)
½ nsec Header

Insertion Loss	from 0.7 to 2.2 db (Figure 19a)
Delay	from 0.47 to 0.81 nsec (Figure 19b)
VSWR	maximum of 1.8 (Figure 19c)

Section 2 (2.5 to 3.5 GHz)
Bit 1 (s/h = 1)

Insertion Loss	from 2.0 to 3.8 db (Figure 20a)
Delay	from 2.2 to 3.3 nsec (Figures 20b)
VSWR	maximum of 2.5 (Figure 20c)

Bit 2 (s/h = 2)

Insertion Loss	from 2.0 to 3.5 db (Figure 21a)
Delay	from 2.1 to 3.3 nsec (Figure 21b)
BSWR	maximum of 2.5 (Figure 21c)

Bit 3 (s/h = 2.5)

Insertion Loss	from 1.4 to 5.0 db (Figure 22a)
Delay	from 2.1 to 3.2 nsec (Figure 22b)
VSWR	maximum of 2.5 (Figures 22c)

Bit 4 (s/h = 3)

Insertion Loss	from 1.2 to 2.5 db (Figure 23a)
Delay	from 2.2 to 2.8 nsec (Figure 23b)
VSWR	maximum of 1.8 (Figure 23c)

Section 3 (2.5 to 3.5 GHz)

Since Sets 1 and 2 of the inductor test pads were used for connecting lumped inductors, these sets will not be discussed as test devices. Instead, the results from the RF chokes which were mounted in them will be presented in their place. Set 3 is an experimental inductor and will be tested and documented as such.

Sets 1 and 2

Figure 24a →	Piconics	M5T47SS (5 turns) + j600 Ω (2.5 GHz) to -j720 Ω (3.5 GHz)
Figure 24b →	Piconics	M20T47SS (20 turns) - j400 Ω (2.5 GHz) to -j200 Ω (3.5 GHz)
Figure 24c →	Piconics	M30T47SS (30 turns) - j250 Ω (2.5 GHz) to -j125 Ω (3.5 GHz)
Figure 24d →	Hand Wound	(10 turns) - j250 Ω (2.5 GHz) to -j125 Ω (3.5 GHz)
Figure 24e →	Hand Wound	(20 turns) - highly sensitive to frequency

Set 3

Figure 25 →	0.5 inches of 1 mil bond wire	+ j80 Ω (2.5 GHz) to -j300 Ω (3.5 GHz)

The test results shown here are a vast improvement over those achieved on Test Circuit I. Insertion loss and VSWR are lower overall, and the time delay is more stable over the frequency range of interest. Also, acceptable results for RF chokes are shown.

First, the insertion loss for the various circuit components is much lower than the losses found on Test Circuit I. The ½ nsec header in Section 1 shows an average loss of 1 db. The losses for the four bits in Section 2 average between

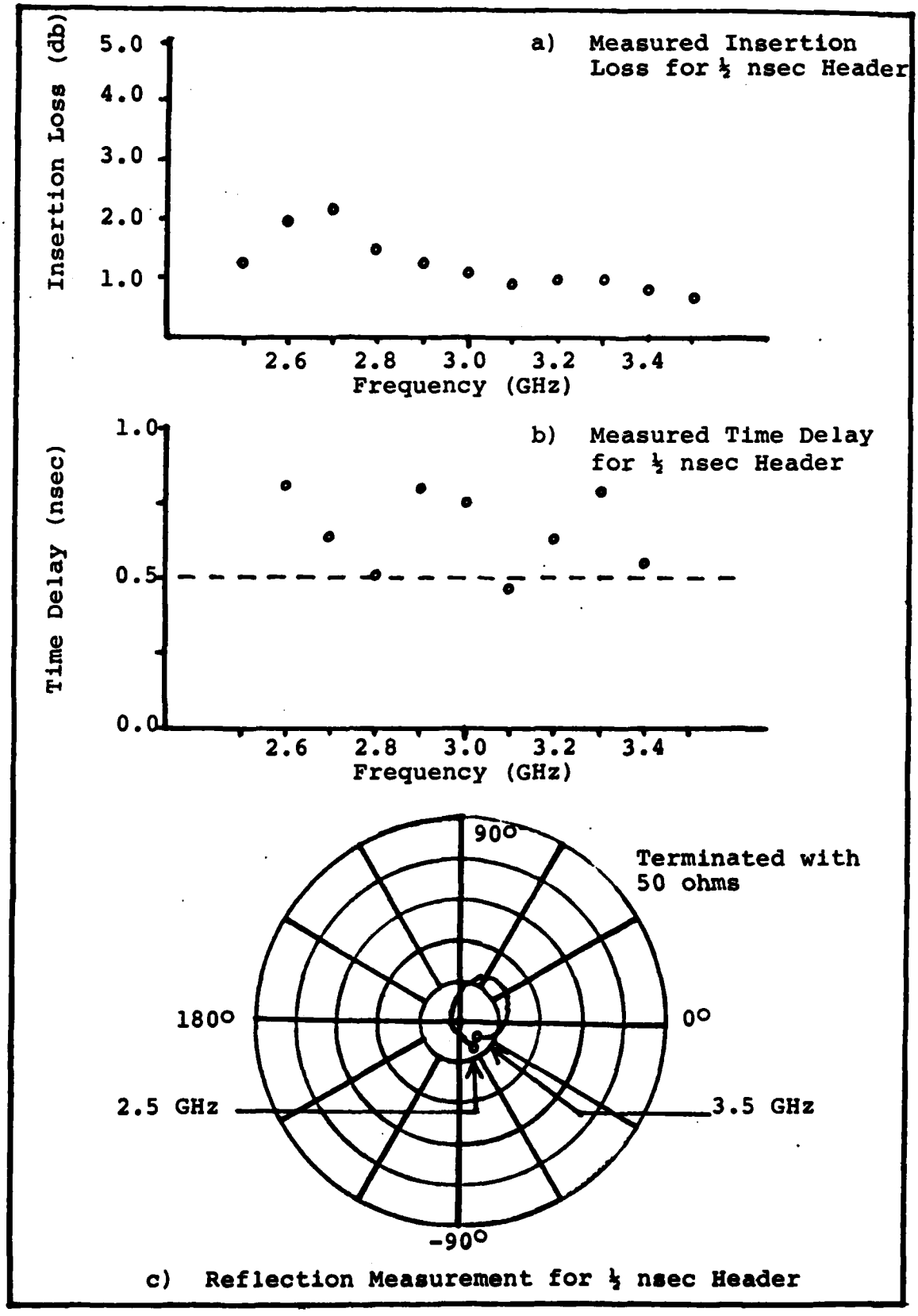


Figure 19. Measured Parameters Versus Frequency of ½ nsec Header on Test Circuit II.

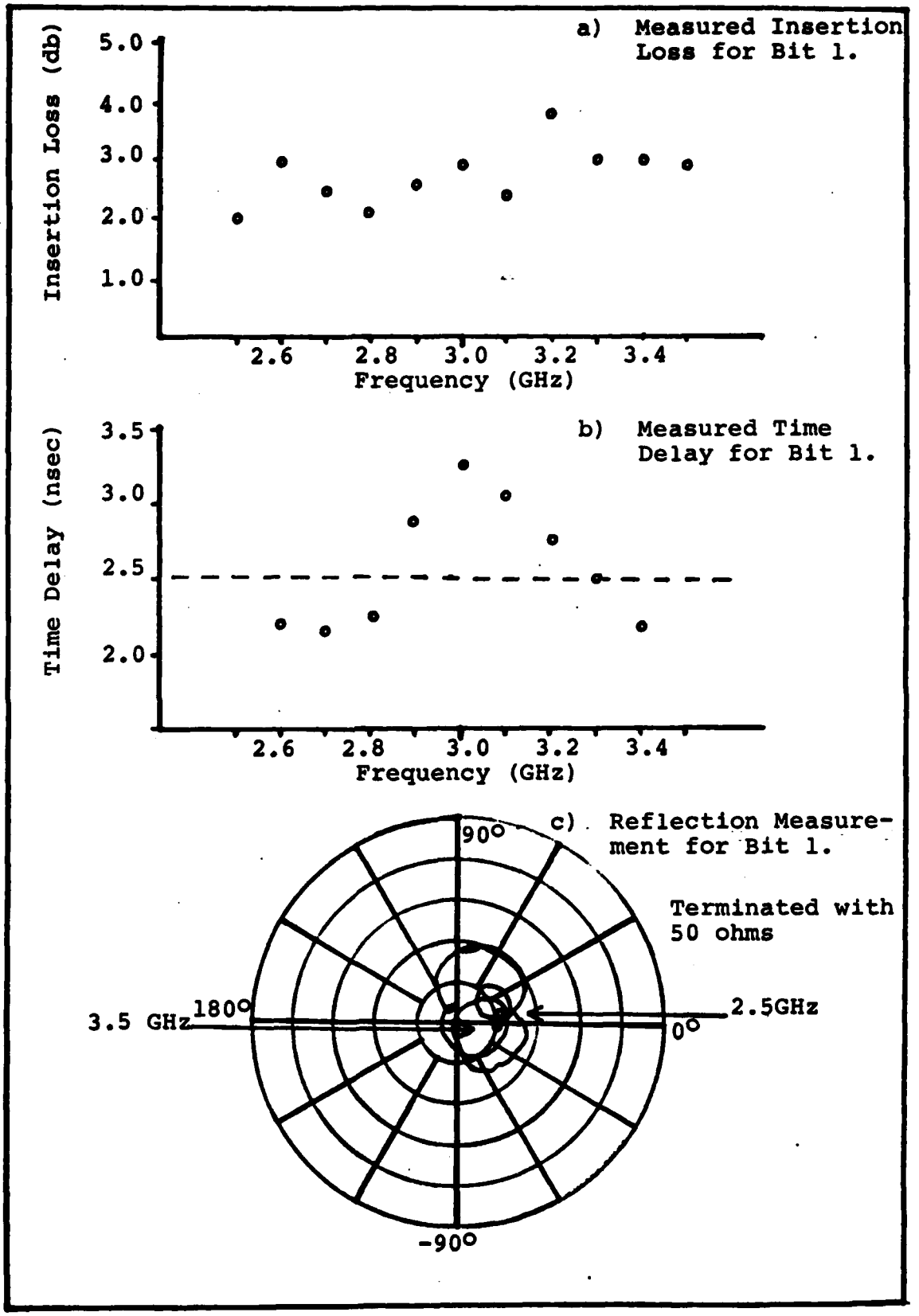


Figure 20. Plots of Measured Parameters Versus Frequency for Bit 1 on Test Circuit II.

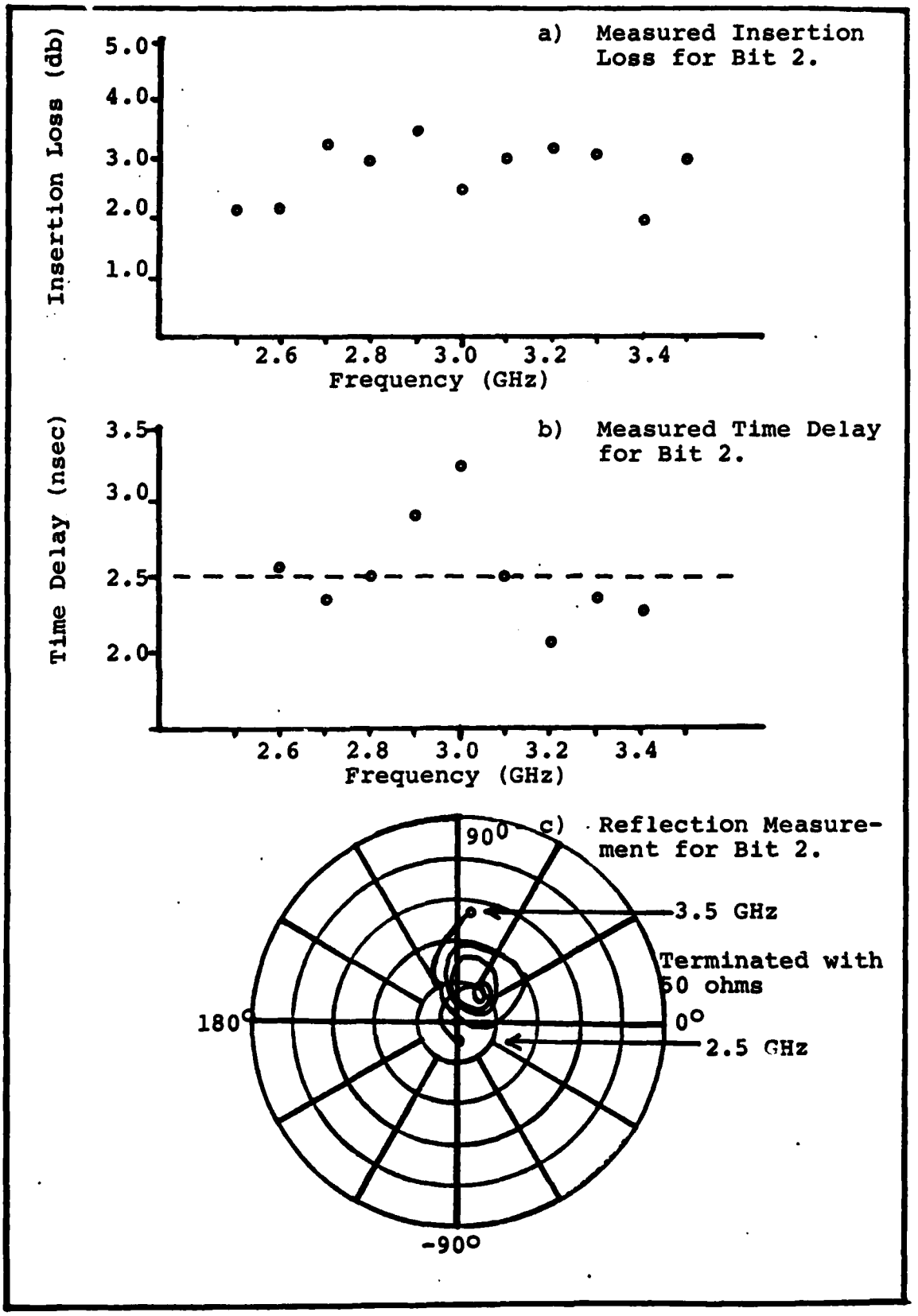


Figure 21. Plots of Measured Parameters Versus Frequency for Bit 2 on Test Circuit II.

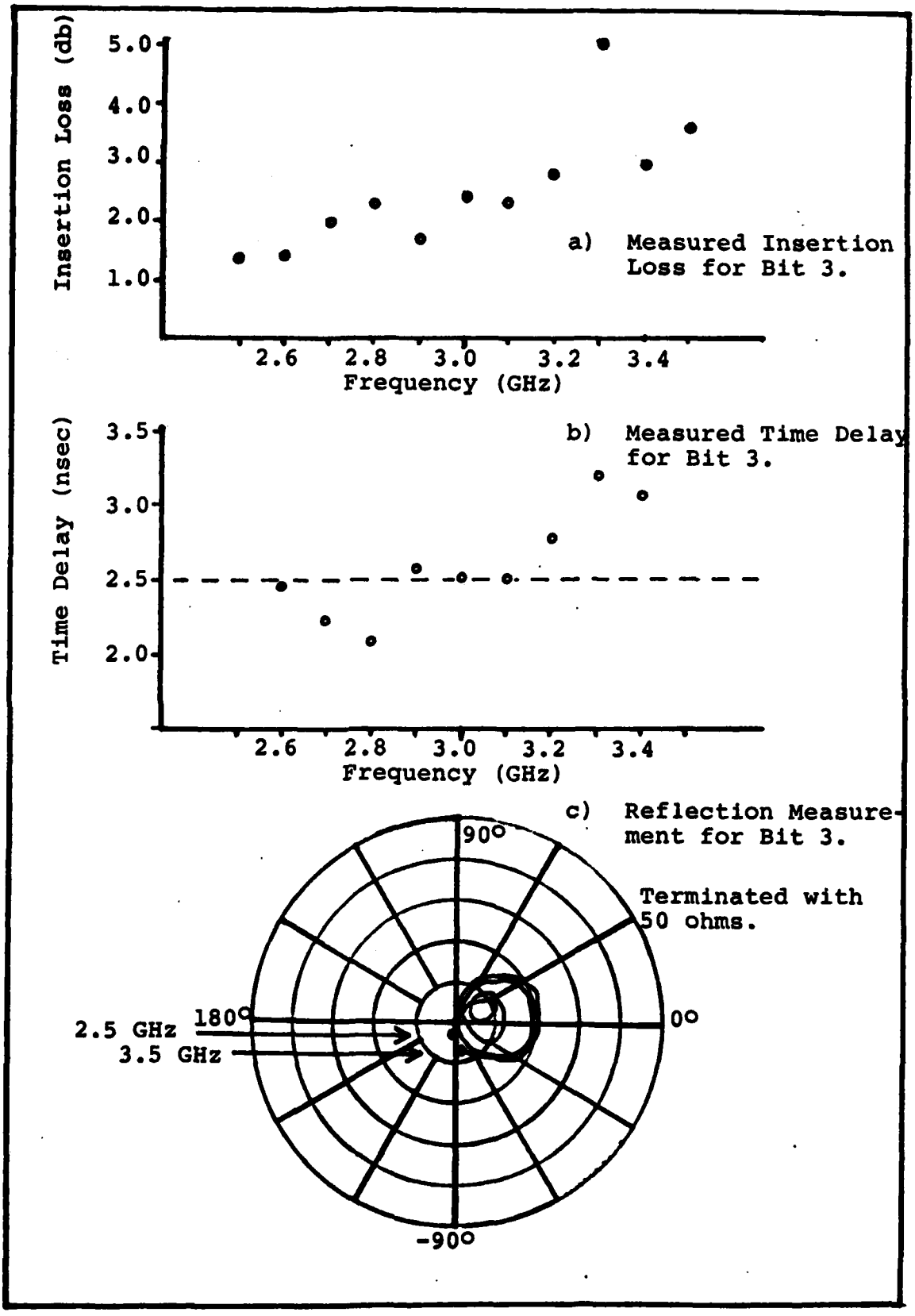


Figure 22. Plots of Measured Parameters Versus Frequency for Bit 3 on Test Circuit II.

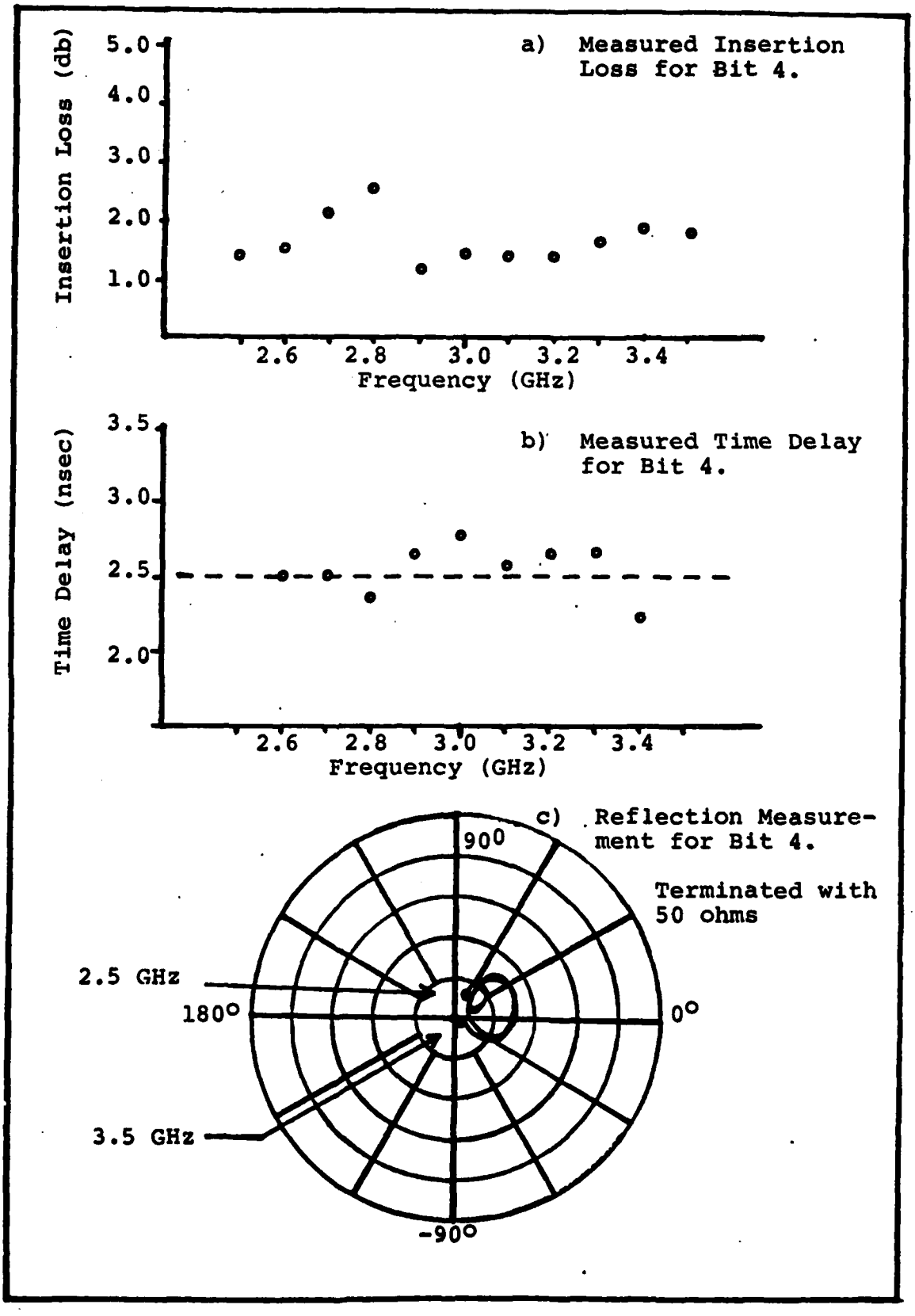


Figure 23. Plots of Measured Parameters Versus Frequency for Bit 4 on Test Circuit II.

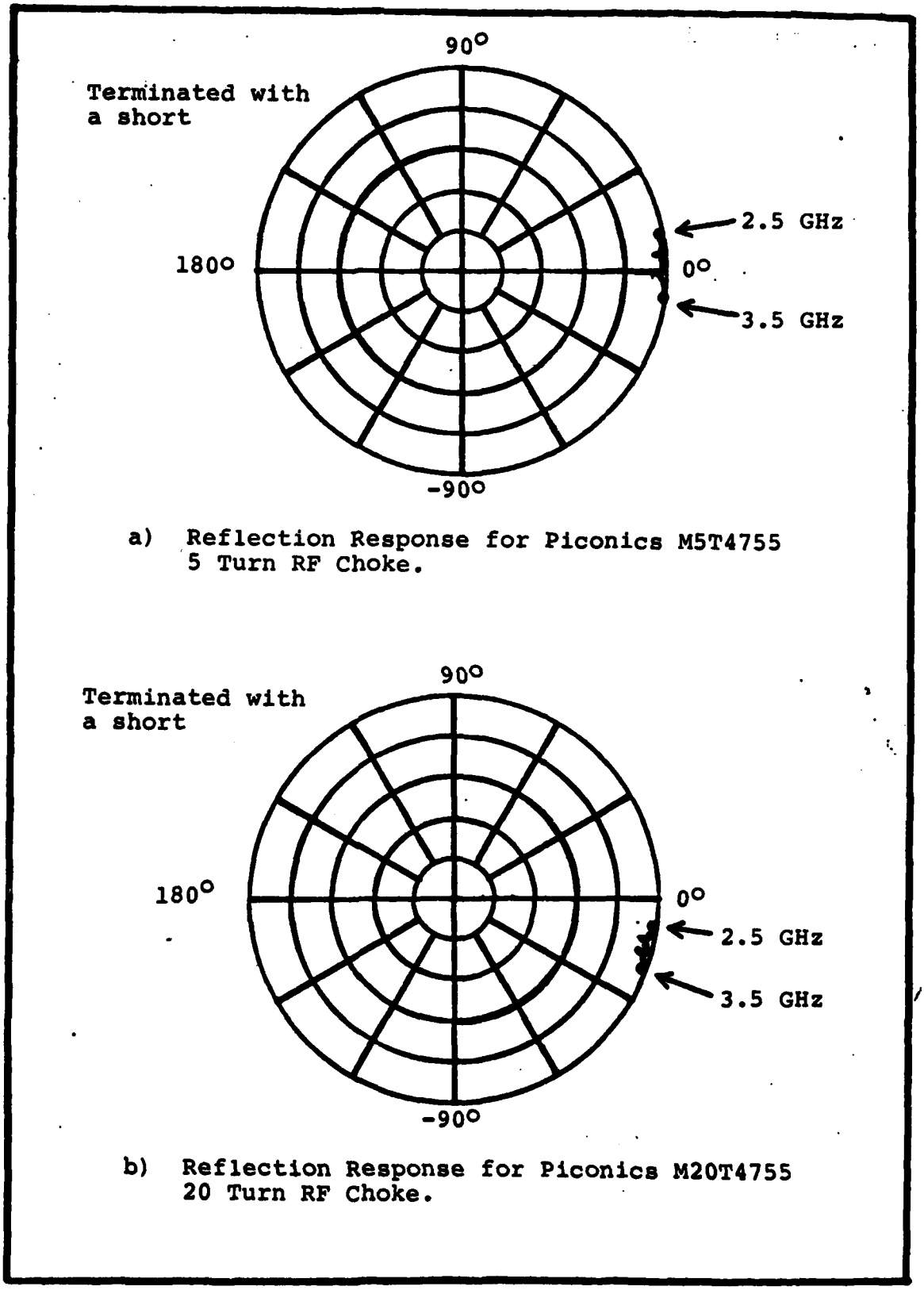
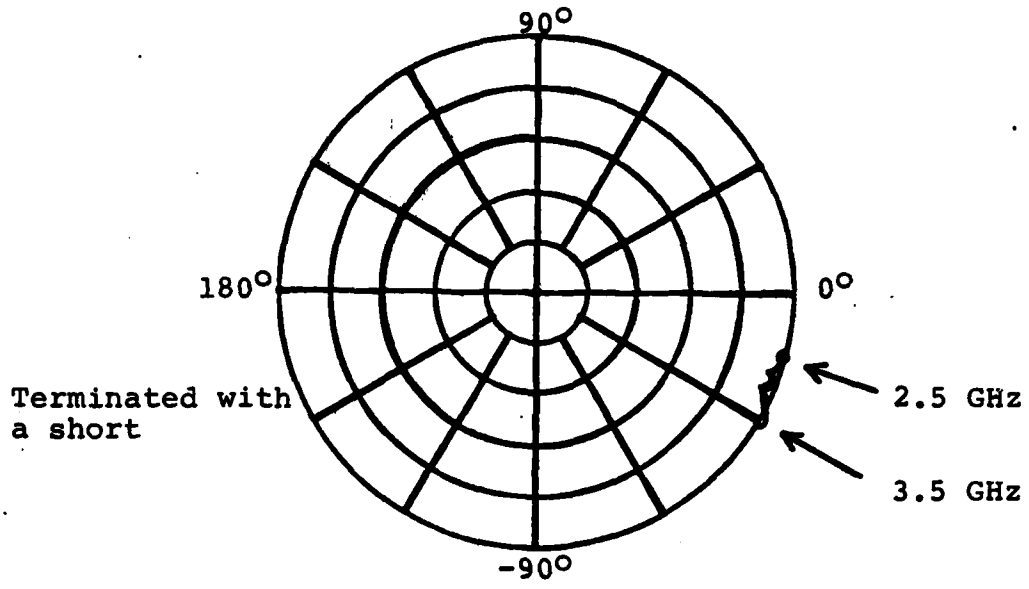
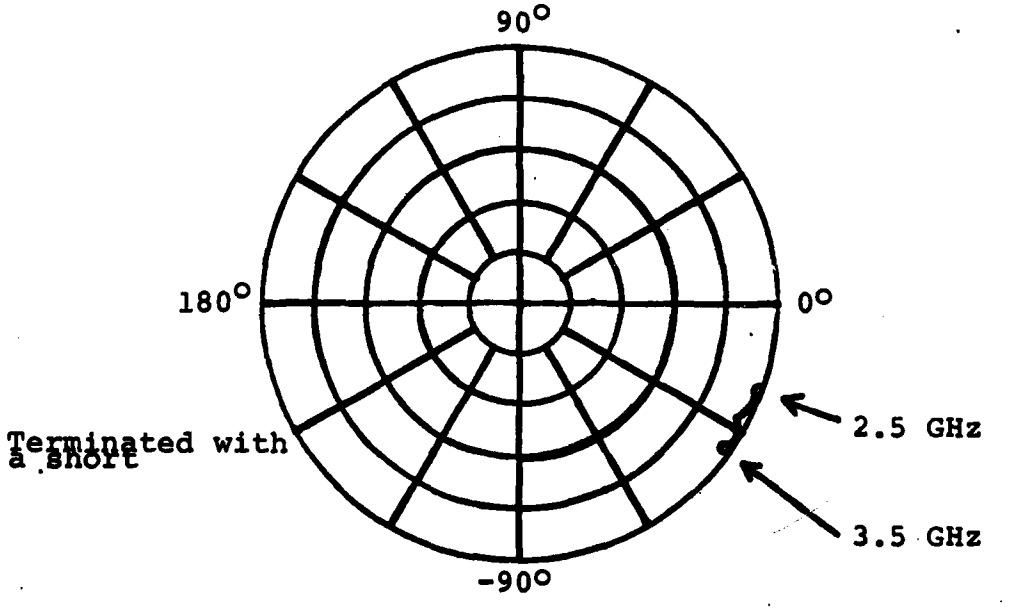


Figure 24. Plots of Reflectometer Output for Wound Inductors on Test Circuit II.

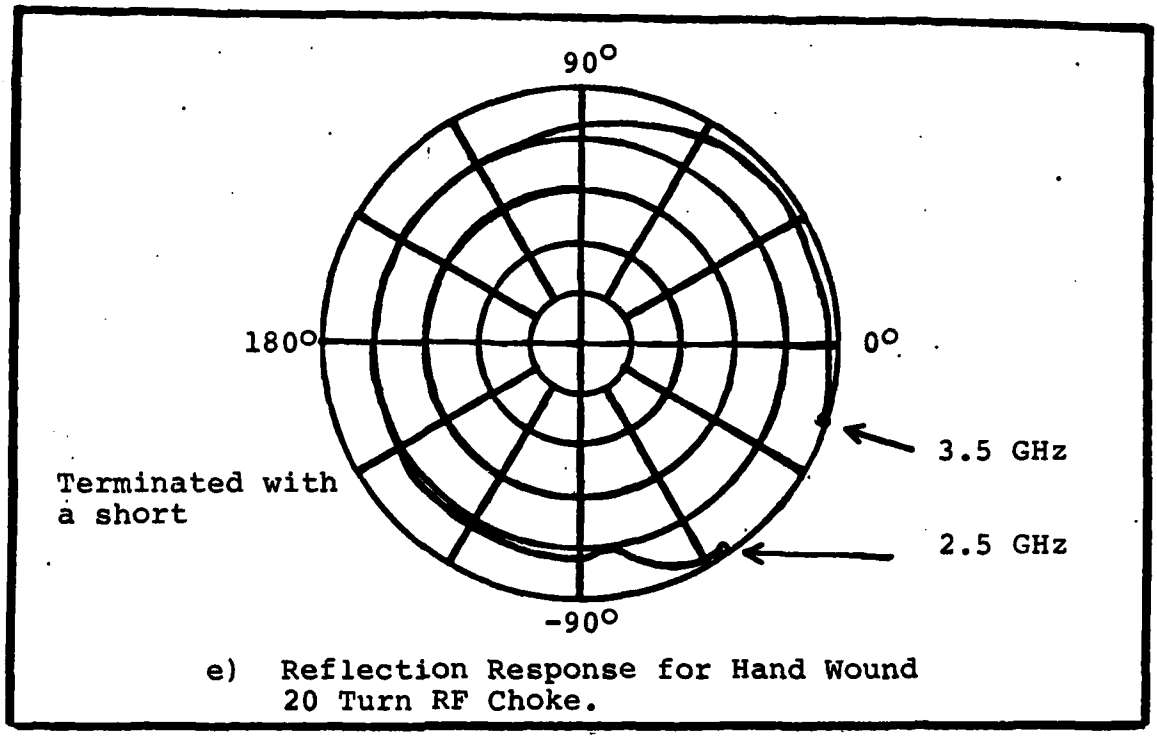


c) Reflection Response for Piconics M30T4755 30 Turn RF Choke.



d) Reflection Response for Hand Wound 10 Turn RF Choke.

Figure 24 (cont.) Plots of Reflectometer Output for Wound Inductors on Test Circuit II.



e) Reflection Response for Hand Wound 20 Turn RF Choke.

Figure 24 (cont.) Plots of Reflectometer Output for Wound Inductors on Test Circuit II.

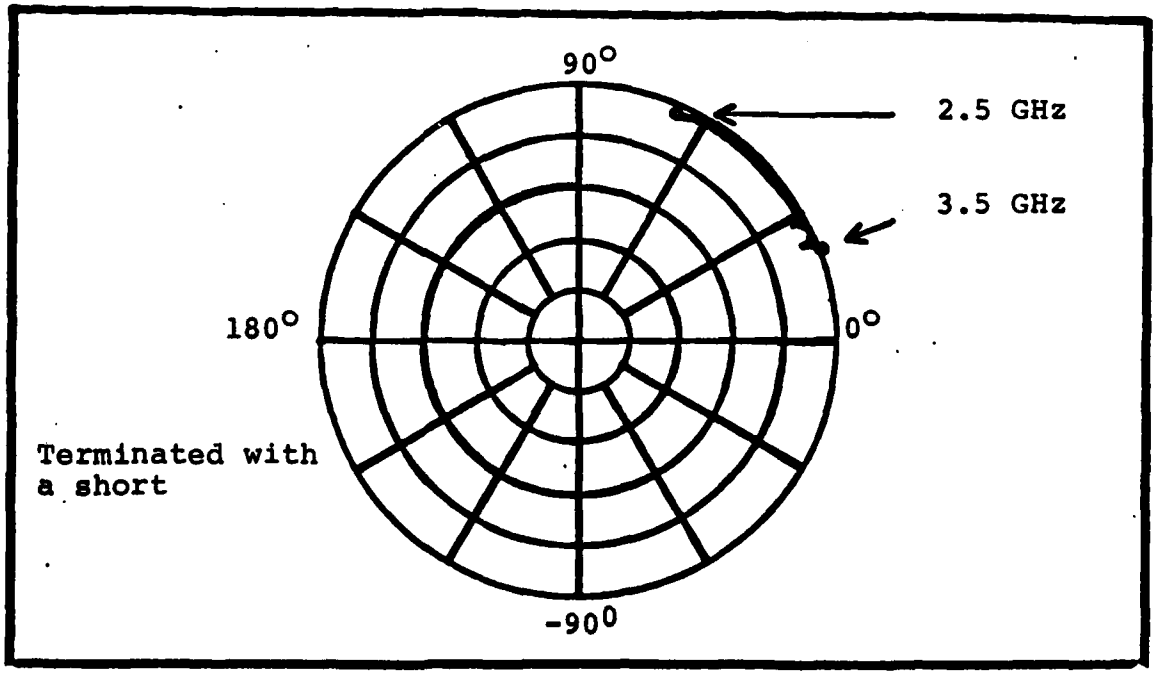


Figure 25. Reflectometer Output for ½ inch long 1 mil Bond Wire on Test Circuit II - Inductor 3.

2 and 5 db. One will note that as the s/h ratio is increased, the average insertion loss for Section 2 decreases.

This inverse relationship also shows up in the VSWR and time delay stability of the circuit components. The VSWR of Section 2 holds at 2.5 for Bits 1,2,3 and drops to 1.8 for Bit 4 (s/h = 3.0). This low VSWR is the same value recorded for the heater in Section 1. Section 2 time delay variations follow this same trend; Bits 1,2, and 3 vary about 45% in time delay over the 2.5 to 3.5 GHz range, and Bit 4 varies only about 25%. Considering insertion loss, VSWR, and time delay variation, an s/h ratio of 3 or greater is acceptable for this TDU design.

Good results were also achieved in the inductor tests. The plots for the five wound inductors tested show their reactance is high and generally is capacitive in the 2.5 to 3.5 GHz range. Figure 26 depicts an inductor model which will help to explain why these inductors appear to be capacitors. (Ref 19:51) L represents the inductor's total inductance, C is the capacitance which occurs between windings and between the device and ground, and R accounts for the inductor's finite conductivity.

Assuming negligible resistance, R, for this discussion, one can show that if the magnitude of the inductor's capacitive reactance, X_C, drops below that of its inductive reactance, X_L, the inductor will appear to be capacitive. If C is not too large, in the desired frequency range X_C will remain comparable in magnitude to that of X_L, and the inductor will maintain a high magnitude of reactance ($|X| \geq 5\ Z_o$). Therefore the

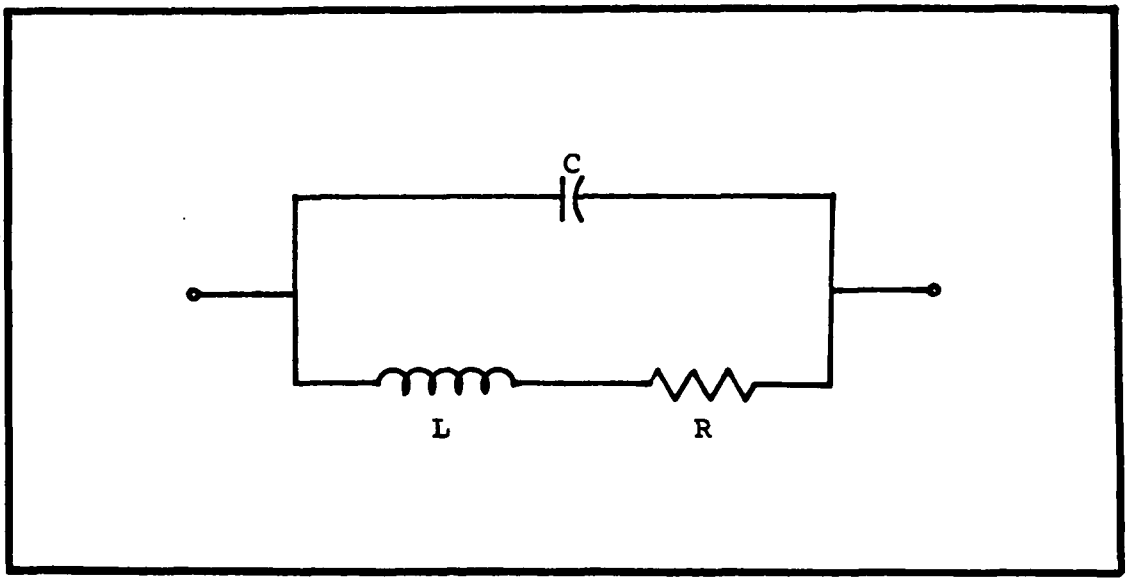


Figure 26. Circuit Diagram of a Model For a Real Inductor. (Ref 19:51)

inductor still serves to block RF voltages and pass dc voltage. This is precisely the case with the tested wound wire inductors. Using X _ 5 Z_o (from -25° to +25° on a polar display) as the requisite for these inductors, the Piconics 5 turn and 20 turn RF chokes show acceptable impedance for this TDU design, and the Piconics 30 turn and the hand would 10 turn RF chokes show marginally high impedance.

In the third set of inductor pads, the 0.5 inches of bond wire proved to be a good inductor, but its impedance is not high enough to work well in this application.

In summary this test circuit has shown that insertion loss, VSWR, and time delay variations are inversely proportional to the s/h ratio of the meander lines in a TDU design. Also, wound wire inductors can be used as the RF chokes needed in the diode control network for a variable delay TDU. The TDU design arrived at with all the above test results is presented in the following section.

IV. Time Delay Unit Design

Introduction

The time delay unit design presented in this section is the culmination of the work performed for this thesis. It is presented as an answer to the circuit requirements listed in Section II of this report. The design details will be shown through a discussion of four aspects of the final design: 1) the substrate, 2) the RF transmission line structure, 3) the diode control network, and 4) the implementation.

The Substrate

Since this is a microstrip design, it is highly dependent upon substrate characteristics. As was shown earlier, the preferred substrate material is $BaTi_4O_9$. The "h" term in the microstrip design equations is 2 mm for the available $BaTi_4O_9$ substrates. Also, the surface area available for microstrip lines is 50 mm by 50 mm. Due to the relatively small area of the substrate, the design goals must be compromised; only a delay range of up to 8 nsec can be made to fit on this substrate. Thus, the final design has a delay range from ½ to 8 nsec in ½ nsec increments.

Other substrate parameters include the very high relative dielectric constant (37.0) and the very low magnitude of its temperature coefficient (-3.67 ppm/^{o}c). The high relative dielectric constant allows the design to be scaled down to relatively small dimensions. On this $BaTi_4O_9$ substrate a 50 ohm line has a calculated width of 0.34 mm, where on the 0.025

inch thick Al_2O_3 substrates the line width is 0.64 mm.

Furthermore, the microwave test fixture shown in Appendix B can be easily altered to make it the size needed for holding the $BaTi_4O_9$ substrate. The base block and ground plane would have to be made narrower - to a width of 50 mm. The same end blocks, however, can be used on either the $BaTi_4O_9$ substrate (2 in. by 2 in.) or the Al_2O_3 substrate (3 in. by 3 in.).

RF Transmission Line Structure

The results of the experiments on the two test circuits show the more efficient TDU design to be the N-bit design. For this reason the final TDU design of this thesis uses the bit structure for the RF transmission lines. The details of the RF transmission line structure are presented in the next few paragraphs.

The $BaTi_4O_9$ substrate for which this design is tailored has a 50 mm by 50 mm surface area. As is noted above, this relatively small area greatly limits the length of transmission line which can be used in the microstrip circuit. Plus allowances must be made for the diode control network. Considering all the limitations, the longest delay which can be fit onto this substrate is 8 nsec. To step through the ½ to 8 nsec delay range in ½ nsec steps, 16 steps are needed. This translates into a 4-bit design. The 5-bit design in Figure 17 can be converted to the desired 4-bit design by removing the longest bit, Bit A, and adjusting slightly the length of all the reamining sections of line. The resulting transmission line configuration is displayed in Figure 27.

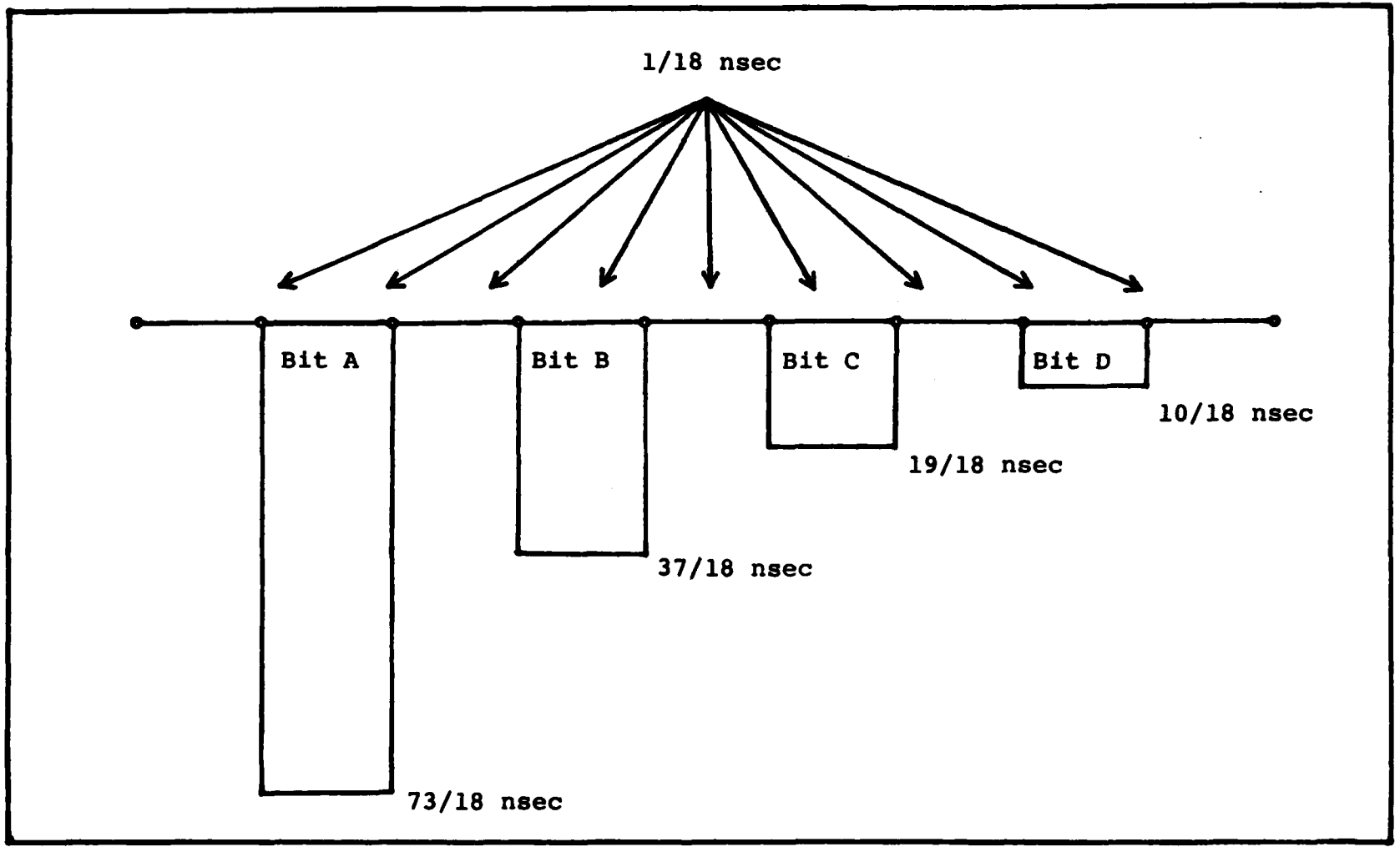


Figure 27. RF Transmission Line Configuration for a 4-Bit ½ to 8 nsec Time Delay Unit.

In order to make the maximum delay 8 nsec, a compromise in one of the design guides suggested earlier must be made. The compromise involves the layout of the two longest bits in the structure, Bit A and Bit B. The transmission line for the longer legs in these two bits has to meander with a relatively small spacing between parallel runs. Although the s/w ratio is equal to 3 for these lines (the same s/w as for the test circuits), the thickness of the substrate (2 mm/0.079 inches) makes the s/h ratio a small value of 0.53. Since the s/w ratio is so large, the effects of the small s/h ratio should not be as severe as those noted for the test circuits.

Diode Control Network

The diode control system for a variable delay time delay circuit is almost as important to circuit performance as the RF transmission line structure. The placement and number of diodes has a direct effect on insertion loss and VSWR. Therefore, three popular schemes were examined before the loaded switched-line design was chosen.

The ideal situation for selecting a path through a bit involves two SPDT switches as shown in Figure 28. By correctly sequencing these switches, one or the other of the lines forms the through-path for the bit. The first approach to this switching problem examined for this thesis was to implement each SPDT switch with two PIN diodes. (Refs 22:392; 11:284) This arrangement is depicted in Figure 29. For ideal diodes this configuration would provide very low losses for the

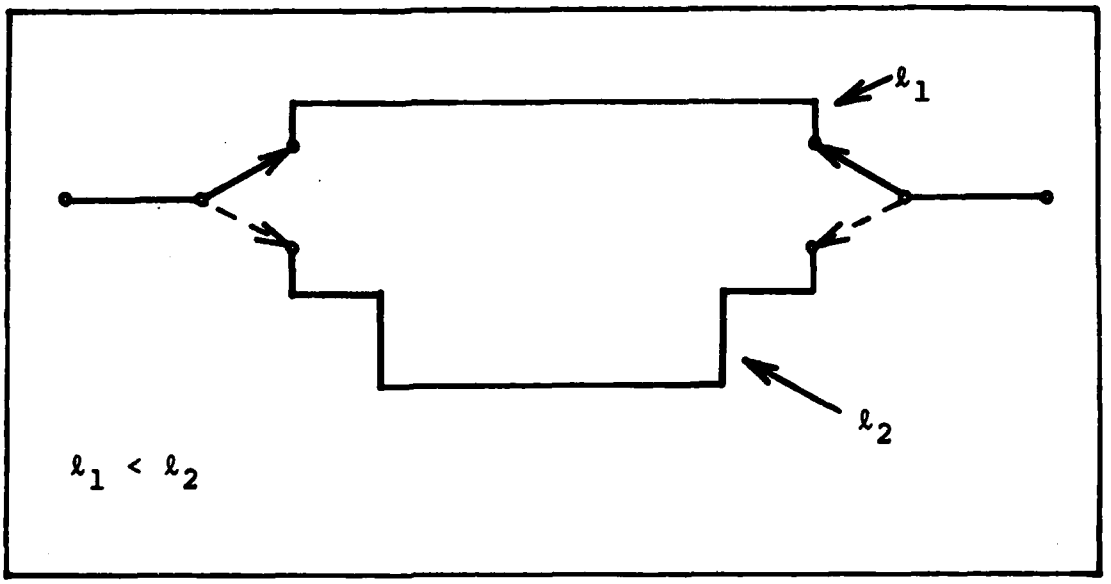


Figure 28. Basic Circuit for Switched-Line or Bit Configuration (Ref 14:693)

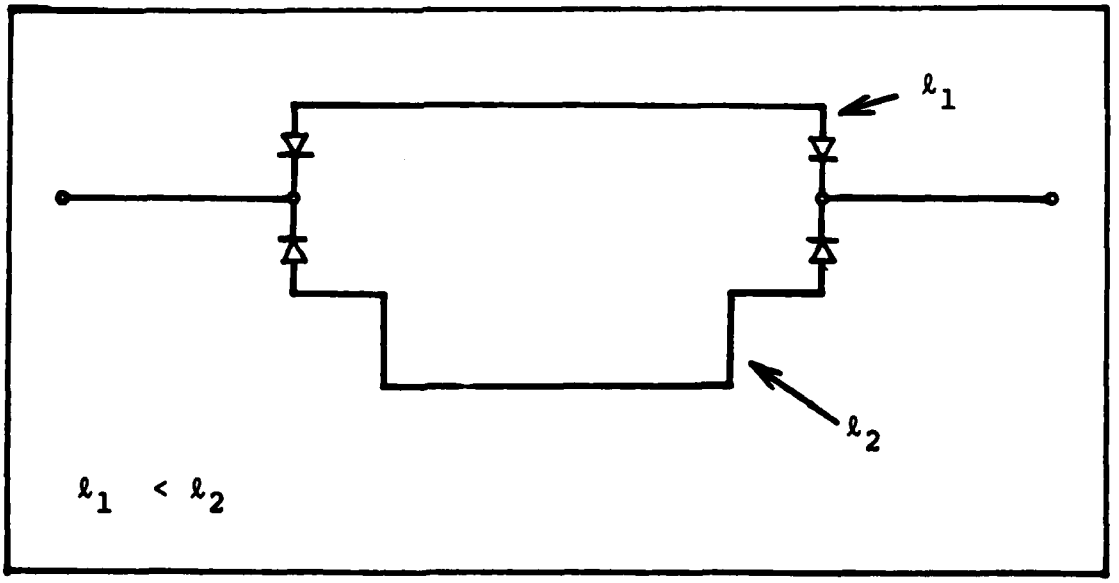


Figure 29. Schematic of Bit Configuration Implemented with Four Diodes (Ref 22:392)

switched in path and very high isolation for the switched out path.

Realistically, this arrangement can yield low loss, a fraction of a db per bit, but only moderately high isolation, generally 20 to 30 db. Two factors contribute to degrading the isolation. The first is the limit to isolation provided by each diode. The second involves resonances in the switched out path. (Refs 14:696; 22:392) If the long path in a bit is longer than $\lambda_m/2$ for the frequency of operation, it can become a resonator. When this path is switched out, a small amount of energy can be capacitively coupled into the line through the reverse biased diodes resulting in a resonance of a frequency which is dependent upon the length of this line. A small fraction of this resonant energy will be coupled out to the rest of the circuit. Figure 30 shows schematically the realistic structure of a bit which uses the simple four diode switched scheme. The amount of coupling depends upon the capacitance of the reverse biased diodes. Nonetheless, the isolation provided by this diode control scheme is adequate but is less than is attainable through other methods. Therefore two other diodes networks were investigated: 1) a modification of this simple scheme and 2) a loaded switched-line network.

The modification to the simple control scheme was the second scheme considered for this TDU design. Instead of just one diode on each end of a long path, this scheme uses two diodes. (Ref 22:400) The isolation provided by each diode adds to increase the total isolation of the long path when it

is switched out. Figure 31 shows this configuration. One problem with the use of the extra diodes is that they are in the RF path, and each diode adds a finite amount of loss and phase shift to the total circuit.

The third scheme, the most electrically complex of the three, employs a different approach for reducing the effects of the resonance of the long path. When the long path is switched out, instead of just removing it further from the rest of the circuit by adding diodes, in this scheme the long path is actually terminated in the circuit's characteristic impedance. (Ref 14:693-697) By loading down the path, any resonance that might occur is effectively dampened. Figure 32a presents a simplistic view of a bit incorporating this loaded switched-line scheme, and Figure 32b shows the full schematic of the network for a 4-bit TDU.

Admittedly, Figure 32b looks very complex, but its operation is not very difficult to understand. All the needed driver circuit parameters are listed in Table III. For these values of resistance TLL levels, and thus TTL circuitry, can be used to drive the switching network. Therefore, controlling the TDU on a gross level is a simple matter. Now to look at its internal operation, only one bit will be examined.

Considering Bit A, if the bit is in its minimum delay state, "A" is high (+5 volts) and "$\bar{A}$" is low (0 volts). The level of "$\bar{A}$" reverse viases D2 and forward biases D3. The D2 diodes block the RF signal from the long path through Bit A, and D3 allows this line to be terminated in 50 ohms (R3).

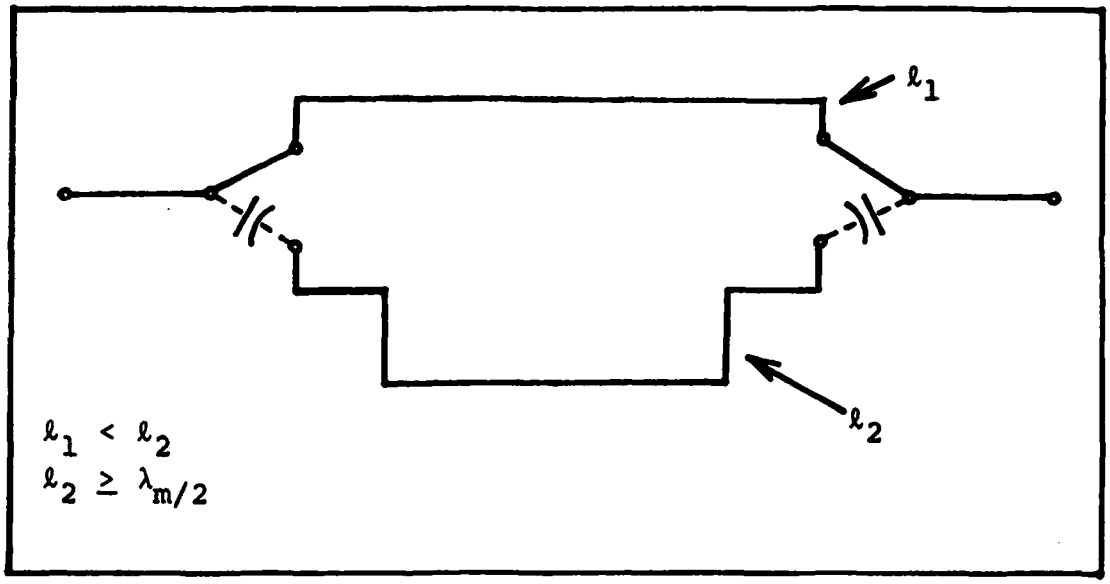


Figure 30. Realistic Basic Circuit for Bit Switch Shown in Figure 29 When Path Length ℓ_1 is chosen. (Ref 22:392)

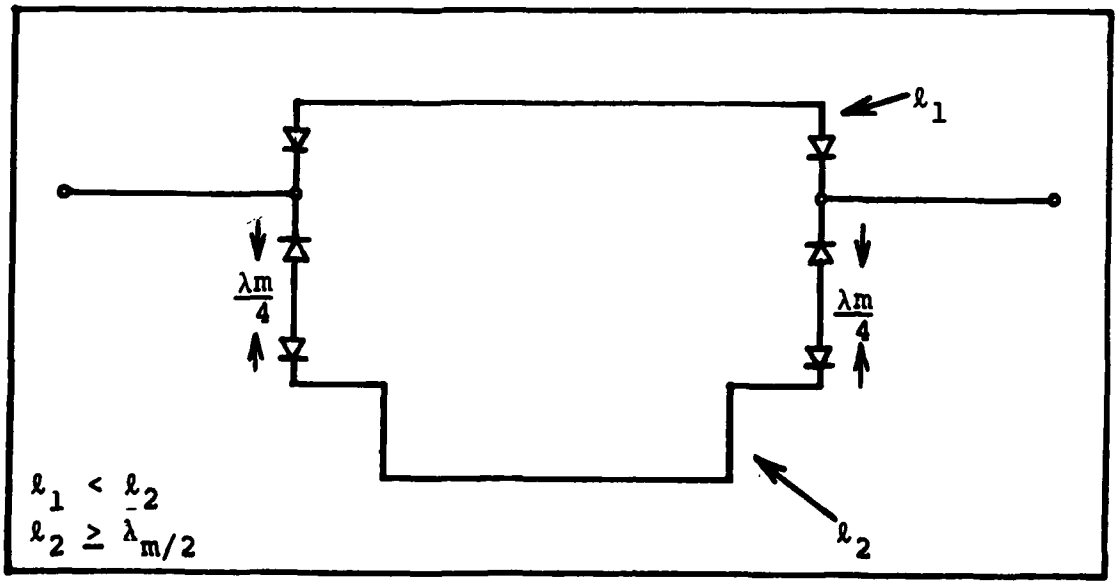


Figure 31. Schematic of Modified Bit Switch Imp'ementation. (Ref 22:400)

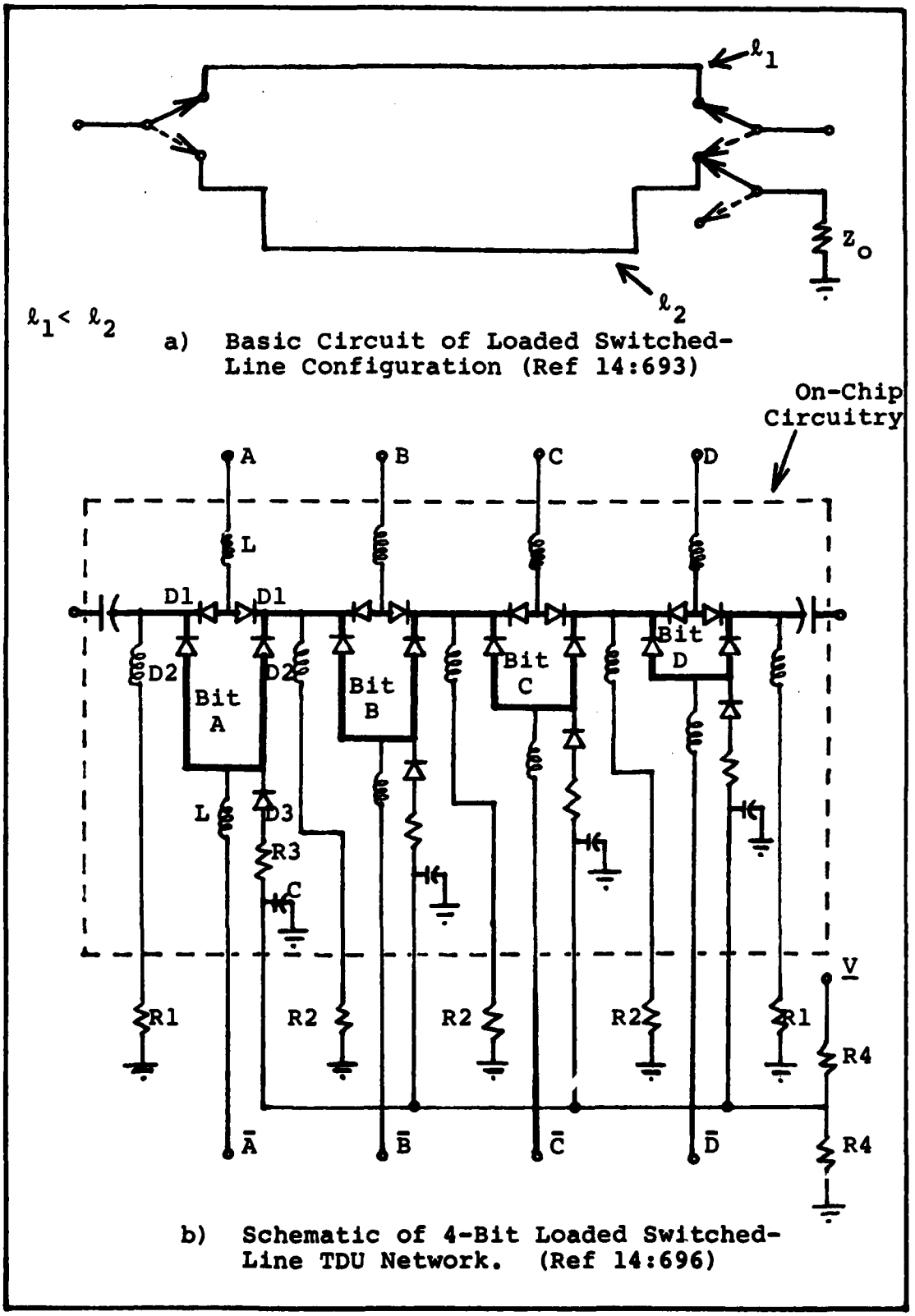


Figure 32. Diagrams of Loaded Switched-Line Circuitry.

Table III. Driver Circuit Parameters for the Loaded Switched-Line TDU Shown in Figure 32b.

Parameter	Value	Units
R1	100	ohms
R2	50	ohms
R3	50	ohms
R4	100	ohms
C	100	pF
L	$\geq$30	nH
V	+5	volts

The level of "A" forward biases D1, and so the RF signal passes through the short path. Current flowing into this path from the control unit through control line "A" is grounded through R1 and R2 which are located on either side of the bit.

In the maximum delay state, "A" is low (0 volts) and reverse biases D1. "$\bar{A}$" is high (+5 volts), and so D2 is forward biased and D3 reverse biased. The long path is no longer terminated in Z_o, and RF signal passes through this leg of the bit. The short leg is nonconductive because of D1.

The scheme of using extra diodes for isolation as in the second approach shown above has been shown to yield good results, but this loaded switched-line network has a couple of advantages over it. (Refs 22:396-397; 14:696) First, in a circuit using the third scheme, fewer diodes are seen by the RF signal when longer delay paths are selected. Therefore, the insertion loss and VSWR are lower. Secondly, since the number of diodes seen is fewer and the VSWR is lower, the time delay stability is improved. For these reasons the loaded switched-line scheme is incorporated into the final TDU design as the diode control network.

Implementation

To implement this circuit, the control schematic of Figure 32b can be easily combined with the RF transmission line schematic of Figure 27 to yield the full TDU layout shown in Figure 33. This layout is dimensioned for a 50 mm by 50 mm by 2 mm $BaTi_4O_9$ substrate but can be adjusted to work on other sizes of substrates.

All circuit components for this design are chip type lumped components. The chip diodes are mounted using the conductive epoxy and bond wire technique described earlier. The chip capacitors can also be attached with this procedure. Chip resistors, however, have both terminals on their upper surface. So they would be affixed to the substrate with insulating epoxy, and then electrically connected to the circuit through bond wires. The inductors selected for this application, the Piconics M5T47SS, are typically self-leaded, unencapsulated wound wire chokes. They can be either soldered or attached with conductive epoxy to the pads provided in the layout.

The final lumped component of the design is the connection to the ground plane. To provide the best possible RF ground, the connection consists of a hole in a metal pad cut through the substrate to the ground plane. This hole is filled with a conductive material (solder, silver paint, etc.) so that the metal pad on the top of the substrate is electrically well connected to the ground plane. Figure 34 depicts the connection of each of these devices.

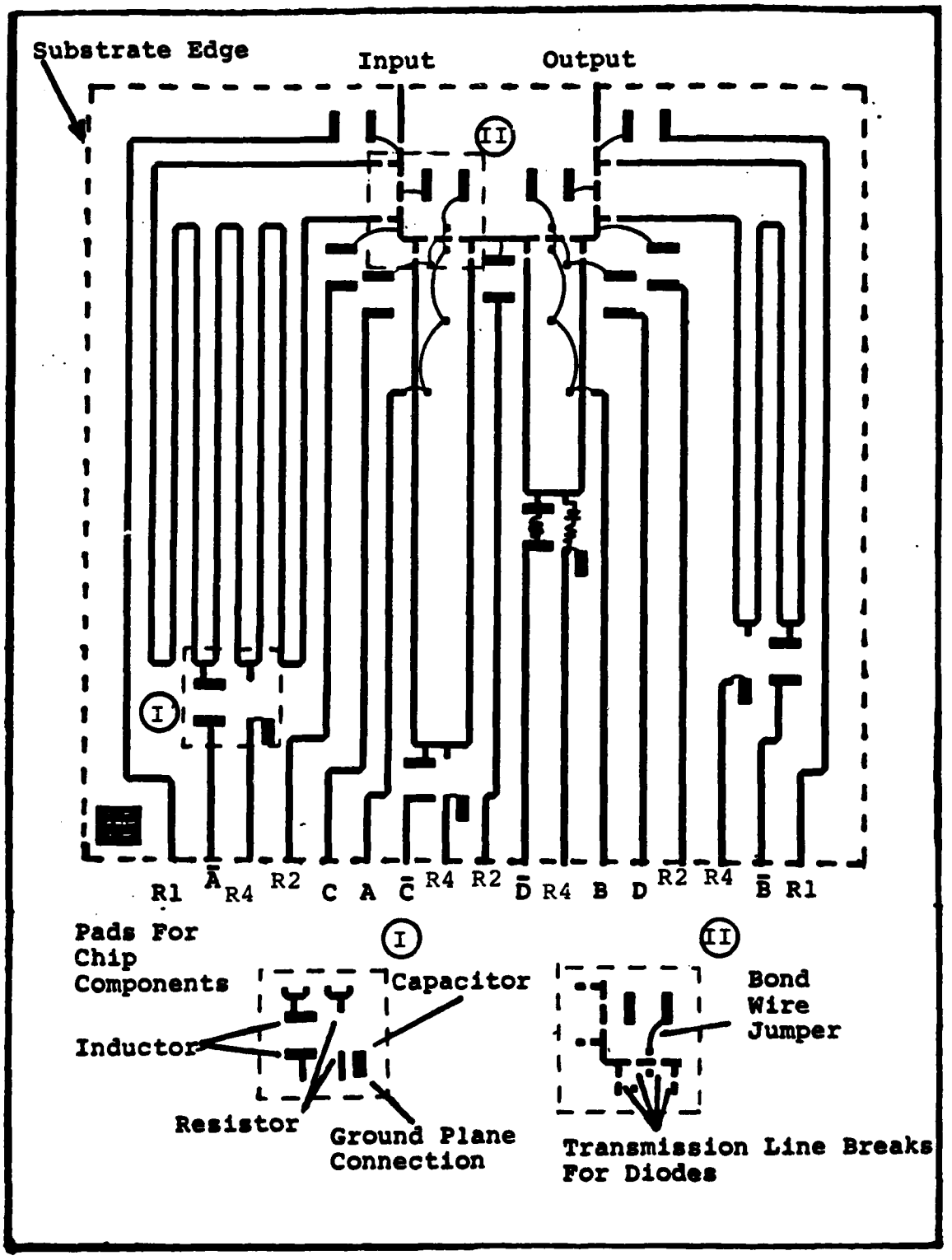


Figure 33. Physical Layout of ½ to 8 nsec Time Delay Unit Designed for 50 mm x 50 mm x 2 mm $BaTi_4O_9$ Substrate.

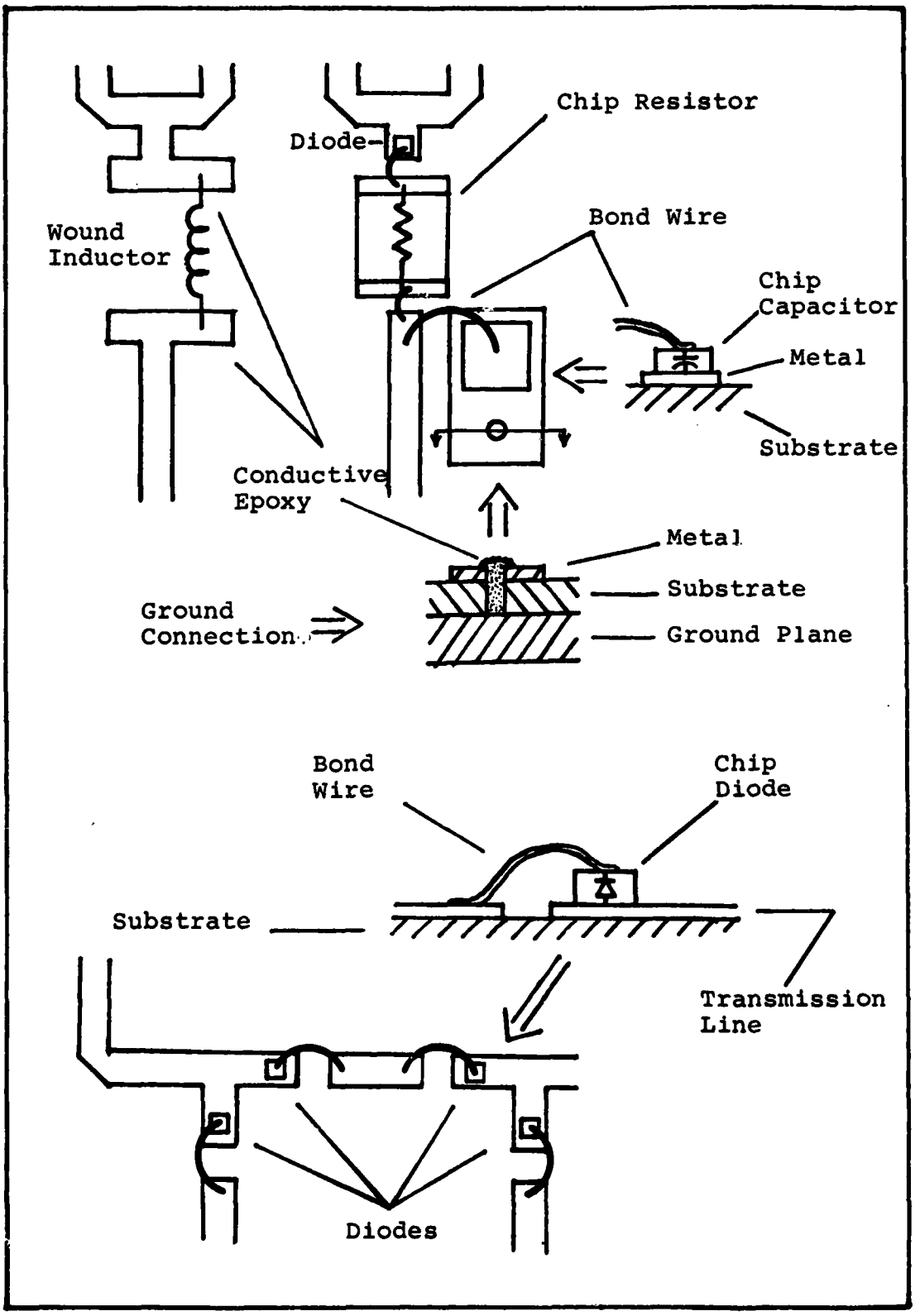


Figure 34. Physical Connection of Lumped Element Components on a Microwave Substrate.

Summary

The TDU design which is the result of this thesis can be described in three sections. First is the $BaTi_4O_9$ substrate for which the circuit dimensions are scaled. The second part is the RF transmission line structure. These transmission lines provide the time delay. The control over the variable delay is supplied by the third major portion of the design, the diode control network. Finally, to simplify implementing the circuit, the design allows all the circuit control components to be composed of lumped hybrid elements - chip diodes, chip capacitors, chip resistors, and wound inductors.

V. Conclusions and Recommendations

Conclusions

In order to improve performance and reduce cost of a phased array antenna, small and easily fabricated variable delay time delay circuits are needed. For this application, microstrip circuit fabrication is the best technique presently in use when miniaturization and ease of construction is considered. Also, although generally the performance of microstrip circuits is not as good as that of bulkier circuits incorporating waveguide or coaxial cable, it is more than adequate. A TDU with a delay range of up to 16 nsec can have an insertion loss of just a few db or less. Microstrip circuits can be produced quickly and easily using thick film or, if necessary, thin film processing steps.

Of the various microstrip substrates available today, $BaTi_4O_9$ has the best combination of characteristics for this application. Its high relative dielectric constant allows circuit dimensions to be scaled to relatively small values, and its low temperature coefficient helps temperature compensate any circuit fabricated on it.

Concerning possible time delay unit designs, an N-bit RF transmission line structure with a loaded switched-line diode control network shows potential as having a very low insertion loss, a low VSWR, and a stable time delay. Furthermore, insertion loss and VSWR of the circuit will be relatively constant across the range of possible delays because of the constant number of diodes seen by the RF signal regardless of

the chosen time delay. Also, the simplicity of the bit structure helps make the circuit design relatively easy to adjust to different sizes and types of substrates. In all, the microstrip design for a ½ to 8 nsec TDU on $BaTi_4O_9$ presented in Section IV of this thesis answers the requirements put forth in Section II.

Recommendations

Although a complete TDU design was produced as an end result of this thesis, further study into a few aspects of this design would help optimize the time delay circuit. Specific recommendations are listed below.

1) Use the mask of the final design produced during this thesis to fabricate and test this design on $BaTi_4O_9$. Temperature cycling should be incorporated into insertion loss, VSWR, and time delay tests.
2) Determine the effects of chip type PIN diodes on an RF signal passing through a 50 ohm line on $BaTi_4O_9$. If the amount of delay added to a line by a diode is known, the length of the line can be adjusted to compensate for this added delay.
3) Investigate other types of inductors for the diode control network. The most promising alternative to wound inductors is printed inductors. Two popular forms of printed inductors are the spiral inductor (Ref 23: 153-156) and the impedance transformer (a form of low pass filter). (Refs 23: 146-147; 1: 107-110)

4) Examine the requirements for a package for a microstrip TDU in its "real world" environment. A small fixture which will take advantage of the small circuit size is needed; yet, the package must provide accurate 50 ohm feedthroughs for the RF signal and must also provide adequate isolation from neighboring circuitry.

Further study in these individual areas of the time delay unit design (diodes, inductors, and the microwave fixture) would help to optimize the RF performance of this circuit. The final results of these studies would be a low loss, low VSWR circuit which could be fabricated relatively inexpensively.

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Appendix A: Test Procedures

Introduction

Throughout this project, the experimental data was measured with a manual Hewlett Packard network analyzer. Figure A-1 shows the hardware and interconnections used. (Ref 2:1.1-1.7) An automatic network analyzer was available, but only on a limited basis. Therefore, only a small portion of data measurement and data verification was done on the automatic system.

In order to characterize the microstrip microwave circuit, four parameters were examined. These are: 1) insertion loss, 2) time delay, 3) VSWR, and 4) impedance. The following sections explain the manner in which each of these was measured. Then a brief overview of the use of an automatic network analyzer is given.

Insertion Loss

Insertion loss is the loss introduced to a system by inserting a device into this system. A comparison of the system with and without the given device under test, DUT, is needed to determine insertion loss. Figure A-2 shows a schematic diagram of the insertion loss measurement set up. With the reflection/transmission test set in the transmission mode, the output signal is the ratio of the reference channel voltage (E_R) to the test channel voltage (E_T).

These two quantities are vectors, so the resultant ratio is also a vector.

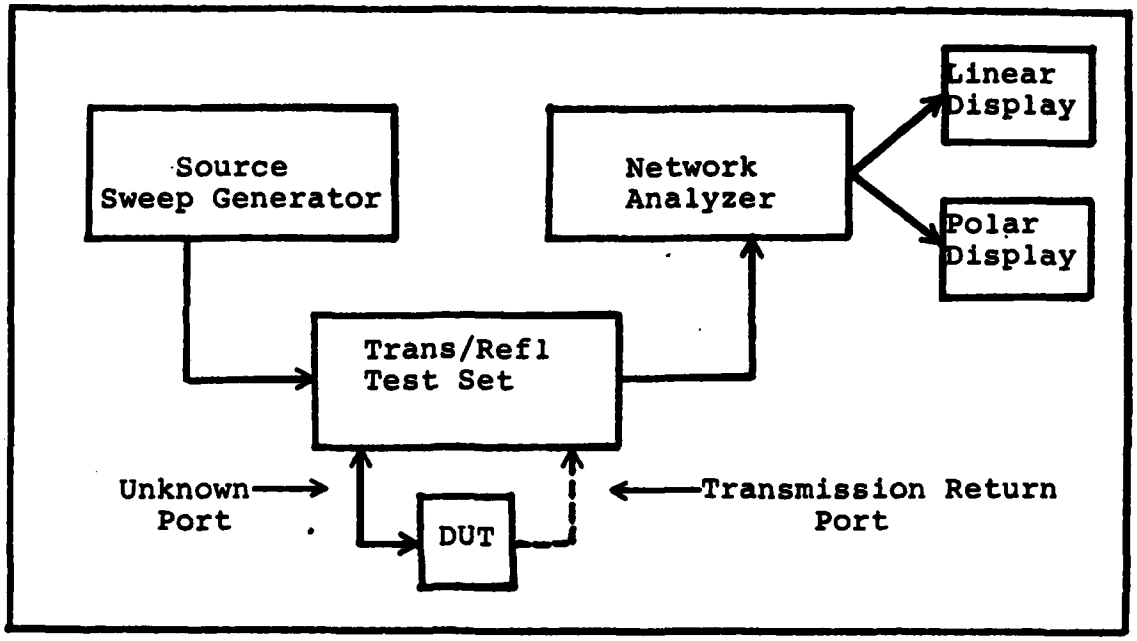

Figure A-1. Hewlett Packard Network Analyzer Hardware Configuration (Ref 2:1-1,1-7)

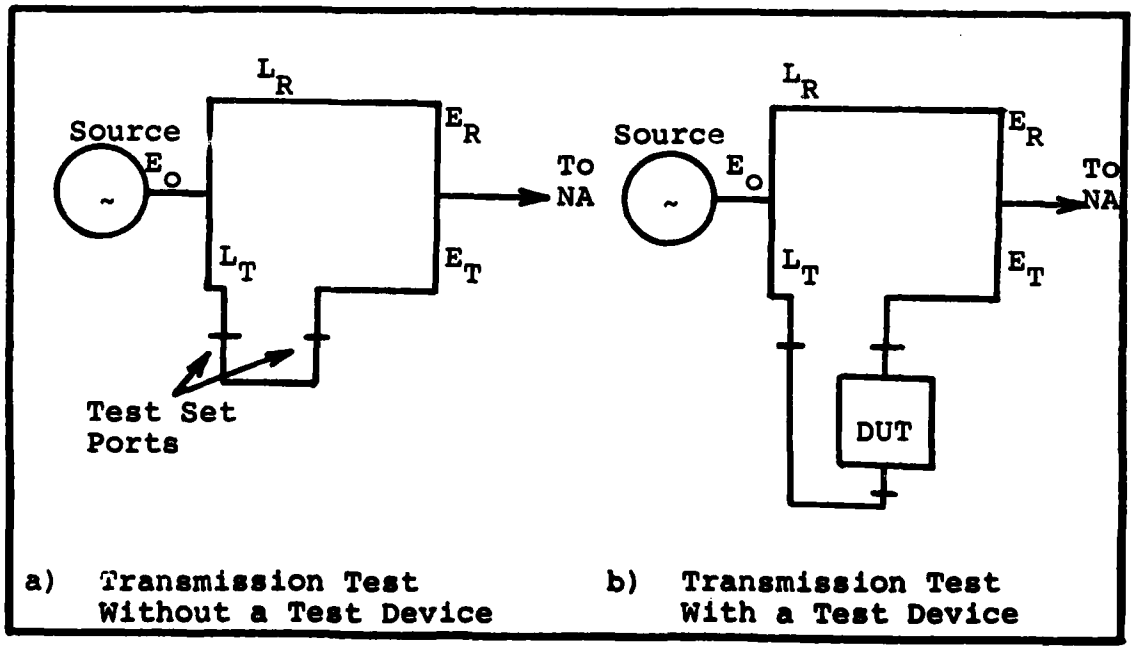

Figure A-2. Schematic Diagram of Transmission Measurement Configurations

$$E_T/E_R = (|E_T|/|E_R|) \quad \angle\phi_T-\phi_R \qquad \text{(A1)}$$

$$\text{Amplitude Response} = 20\ \text{Log}_{10}\ (|E_T|/|E_R|) \qquad \text{(A2)}$$

$$\text{Phase Response} = \phi_T-\phi_R \qquad \text{(A3)}$$

Insertion loss in decibels is derived directly from (A2):

$$\text{Insertion Loss (db)} = 20\ \text{Log}_{10}\ (|E_T|/|E_R|). \qquad \text{(A4)}$$

This quantity in db may be displayed directly on the NA's linear display for the range of frequencies chosen on the sweep generator. Insertion loss versus frequency can be read directly from the NA display by using the following procedure. To calibrate the display for a specific cable and frequency, the cable must be connected between the two test set ports, and resultant amplitude response recorded. This display can be recorded with either a pen plotter or on film. Next the DUT is connected between the "unknown" port on the test set and the end of the cable which was previously connected to this port. The trace now displayed shows the summed insertion loss of the DUT and the cable connecting it to the "transmission return" port. The insertion loss of just the DUT can be found by recording this display and subsequently subtracting it from the previous display.

Time Delay

The amount of time needed for a RF signal to travel from the input port to the output port of a device is that device's time delay, or group delay (τ). This characteristic is of prime importance for a time delay circuit.

Group delay is found through a calculation performed on the device's transmission phase response. Below is the theoretical derivation of the τ equation followed by the procedure for finding the time delay for a given circuit.

In Figure A-2, L_T and L_R are the electrical lengths in meters of the test and reference channels, respectively. As shown in (A1) the theoretical representation for E_T and E_R is

$$E_T = |E_T| \angle\phi_T \tag{A5a}$$

and

$$E_R = |E_R| \angle\phi_R, \tag{A5b}$$

where

$$\phi_T = \beta L_T = (\omega/v) L_T = (L_T/v) \omega, \tag{A6a}$$

$$\phi_R = \beta L_R = (\omega/v) L_R = (L_R/V) \omega, \tag{A6b}$$

(Ref 9:107, 19:111) and the group delay of a signal through each of the channels can be shown as

$$\tau_T = L_T/v \tag{A7a}$$

and

$$\tau_R = L_R/v. \tag{A7b}$$

As stated in (A3) the phase response shown on a NA is $\phi_T - \phi_R$. This expression is equal to

$$\phi_T - \phi_R = \phi_D = \omega (\tau_T - \tau_R) \tag{A8}$$

Here ϕ_D equals the difference between ϕ_T and ϕ_R. For the lengths L_T and L_R, three possible cases exist.

$$\text{Case I} \qquad L_T = L_T \tag{A9a}$$

$$\text{Case II} \qquad L_T > L_R \tag{A9b}$$

$$\text{Case III} \qquad L_T < L_R \tag{A9c}$$

For the purposes of these measurements, only case I and II

are of interest.

For ϕ_D versus frequency, as is the case for phase response on a NA, the slope of a line in this system would be $d\phi_D/d\omega$. As can be seen from (A8),

$$d\phi_D/dw = (L_T - L_R)/v, \tag{A10}$$

and

$$d\phi_D/dw = (L_T - L_R)/v. \tag{A11}$$

Combining (A7) and (A11) yields

$$d\phi_D/d\omega = \tau_T - \tau_R = \tau_D \tag{A12}$$

where τ_D is the difference in time delay between the test and reference channels. So (A12) shows the differential time delay of the two channels is directly related to the slope of the phase response.

For case I, τ_D is zero, meaning that the two channels are of the same electrical length. This case corresponds to a phase response display of a horizontal line on a NA.

Now for case II, τ_D has a nonzero value representing the difference in time needed by a signal to travel through the two channels. On a NA case II is seen as a sloped line. By measuring $d\phi_D$ in radians and dw in radians per second from this sloped line, τ_D can be determined through (A12).

This information can be readily obtained from a NA. First, a cable must be connected between the two ports on the test set as in Figure A-2a. Then L_R is adjusted by turning the dial on the front panel of the test set until the trace representing the transmission phase response becomes a horizontal line. This situation corresponds to

$L_T = L_R$. Now the DUT is inserted into the test channel as in Figure A-2b. The quantity $d\phi_D$ can be read from the display in degrees, and df in hertz. After converting $d\phi_D$ to radians and df to dw, one can substitute these values into (A12) yielding τ_D. Since τ_T was equal to τ_R before the device was inserted, this value of τ_D represents only the time delay of the DUT. Therefore, τ_D is equal to the average time delay of the given device in seconds over the frequency range scanned in df.

VSWR

The voltage standing wave ratio, VSWR, for a given circuit is important because it shows how well the device's impedance matches that of the rest of the system. VSWR is a funtion of the voltage incident upon a device (E_I) and the voltage reflected from that device (E_{RL}).

$$VSWR = (E_I + E_{RL})/(E_I - E_{RL}) \qquad (A13)$$

For taking reflection measurements, a reflectometer such as the system shown in Figure A-3 is needed. A reflectometer consists of a sweep generator connected to the DUT with this device terminated in Z_o. Additionally, highly directional couplers sample the incident voltage and the reflected voltage. Using this setup the VSWR of a device can be easily determined on a NA.

The first step in making a VSWR measurement is to calibrate the polar display of the NA with respect to amplitude using a 50 ohm load and a short. This procedure is well documented in all NA manuals. Therefore, it will

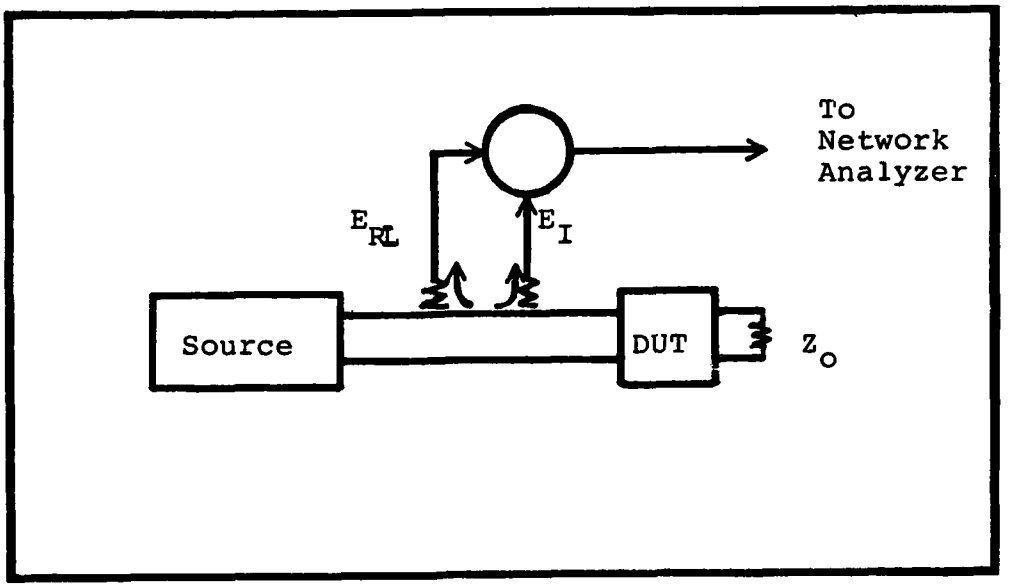

Figure A-3. Block Diagram of Reflectometer Setup (Ref 2:1-1,1-7)

not be discussed here. Next, the input port of the DUT is connected to the "unknown" port of the test set, and the DUT's output port is terminated in Z_o.

At this point, the trace on the polar display is a spiralling line segment whose length is dependent upon the range of frequencies selected on the source (sweep generator). Taking the center of the polar display as a value of zero and its outer rim as one, the maximum radius of this circular trace must be determined. This radius, which has a magnitude between zero and one, is the magnitude of the reflection coefficient, $|\rho|$. By using this value of $|\rho|$ in (A14), the maximum VSWR for a given device within the swept frequency range is derived. (Ref 11:200)

$$VSWR = (1 + |\rho|)/(1 - |\rho|)$$

AD-A124 754 S-BAND VARIABLE TIME DELAY CIRCUIT ON BARIUM TETRATITANATE(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGINEERING 2/2

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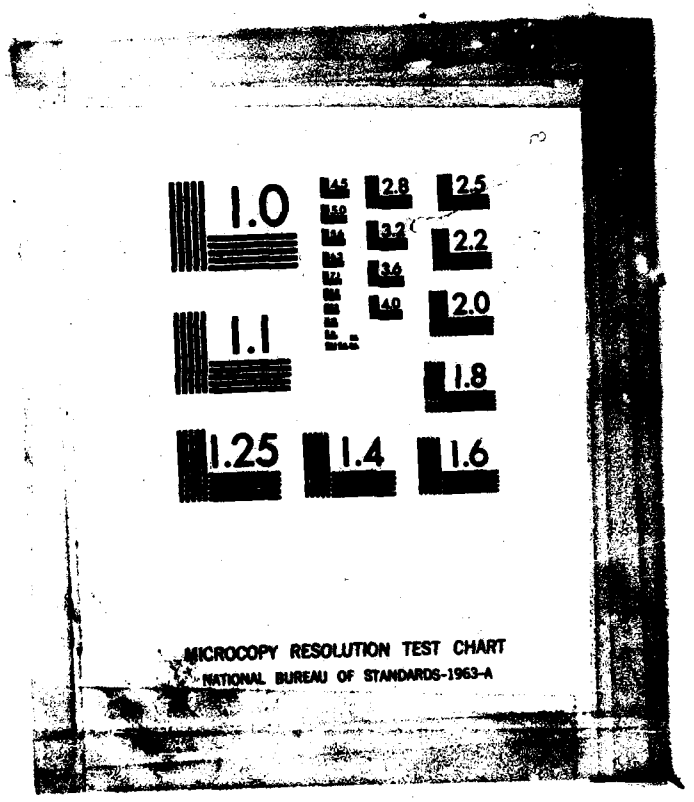
1.0
1.1
1.25
1.4
1.6
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.8
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

Impedance

The fourth parameter of interest for this project is inpedance. The impedance of an RF choke is especially important and will be used as an example. An RF choke must have very high reactance to prevent an appreciable amount of RF power from draining into the dc power supply used for biasing diodes.

The procedure for measuring impedance versus frequency of an RF choke is relatively simple. First, the NA is calibrated using a 50 ohm load and a short. Next, the DUT is connected to the "unknown" port of the test set as in Figure A-3 and terminated with a short circuit. With the source set to sweep the frequency range of interest, the RF choke should yield a trace on the polar display which closely follows the outer rim (low resistance) and is in the $\pm$ 40 degrees region (high reactance). With a Smith Chart overlay on the display, the device's normalized impedance can be read directly from the display. The actual impedance is derived by multiplying this value by Z_o.

Automatic Network Analyzer

An automatic network analyzer (ANA) is an extremely complex device. It is, however, relatively simple to operate. The ease of operation arises from the fact that it is computer driven, and the interfacing computer program is very user oriented.

A typical measurement cycle on an ANA consists of calibrating the setup, connecting the DUT, and running a

series of tests. For calibration, the ANA requests the user to connect certain devices such as a calibrated short, open, and sliding load. It performs tests on each device and stores the data. Then the DUT is connected, and the ANA performs transmission and reflection tests on it. After the tests are done, the ANA subtracts out the losses and VSWR added to the test system by the connecting cable. Thus, the characteristics for a device given by an ANA are relatively easy to derive and can be very accurate.

Conclusion

Through the parameters listed above, the test circuits and individual circuit components for this project were analyzed. The measuring techniques were arrived at through consultations with Capt R. Colvin and Mr. M. Calcattera, and the procedures have proven to be accurate and repeatable.

Appendix B: Microwave Circuit Fixture

In this appendix the design of the test fixture for holding the microstrip circuits is presented. The design was adapted from one provided by Captain Colvin which is used for x-band testing of GaAs MESFETs. A picture of the fixture used for this thesis is displayed in Figure B-1.

The basic fixture consists of four parts: The base block, the ground plane, and the two end blocks. The base block is an aluminum block onto which the other parts are attached. The ground plane is a gold plated sheet of brass which is placed on top the base block, and the microstrip circuit goes on top the brass ground plane. The end blocks are gold plated pieces of brass that bolt onto opposite sides of the base block. Feedthrough pins protruding from the inner side of the end blocks put pressure on the microwave circuit substrate, holding it and the ground plane firmly down against the base block. The pins also provide the electrical connections to the circuit by resting on microstrip lines.

The adaptation of the fixture for this thesis consisted of three major changes. First, the fixture was scaled up large enough to hold a 3 inch by 3 inch substrate. The second change involves putting both the input and output RF feedthroughs on the same end block instead of the typical configuration of one on each block. The setup used here allows a feedthrough separation distance from 1/2 to 2 1/2 inches. The 1/2 inch separation permits the circuit

designer to use a short line length between the input and output feedthroughs. Thus, the minimum total inserted delay can be very small. End block is shown in Figure B-2.

The third change consists of locating a fifty pin wire wrap connector on the other end block, the one opposite from the RF feedthrough end block. Half of the pins were removed so only twenty-five pins protrude through the end block and make contact with the microwave circuit. These pins provide the diode dc control voltages necessary for switching the delay of the TDU. Figure B-3 shows this end block.

Figures B-4 and B-5 show the last two of the four parts of the fixture, the brass ground plane and the aluminum base block. Separate ground plans and baseblocks were made for the two substrate materials since the substrates were different in size. The same end blocks, however, can be used with either size substrate.

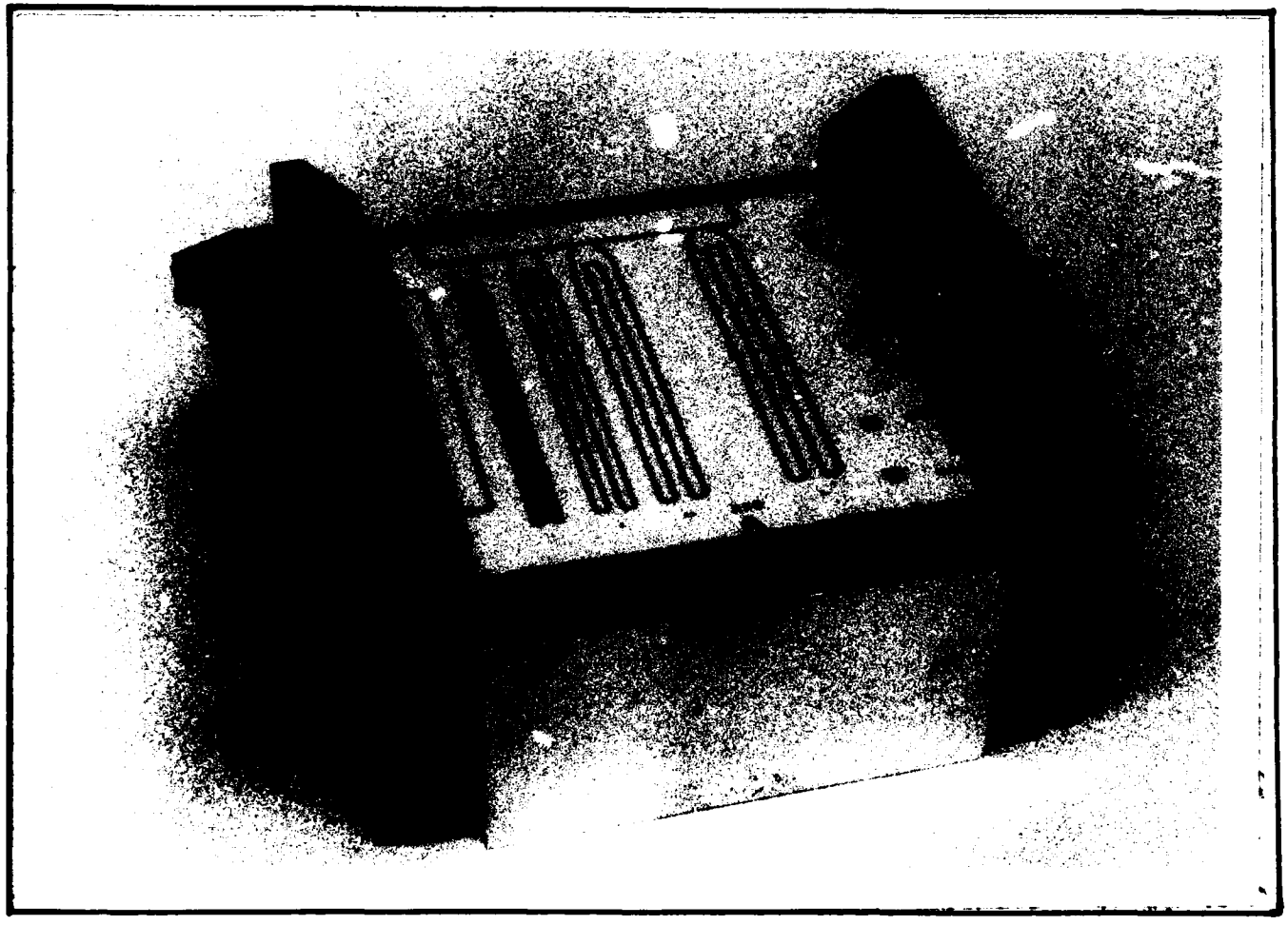

Figure B-1. Microwave Test Fixture.
Test Circuit II is shown.

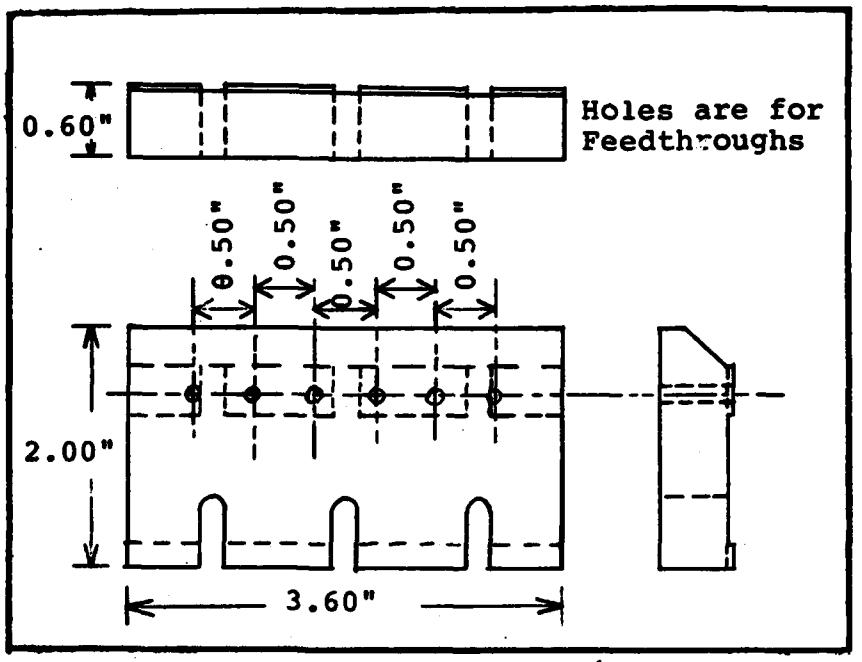

Figure B-2. RF Feedthrough End Block (Gold Plated Brass)

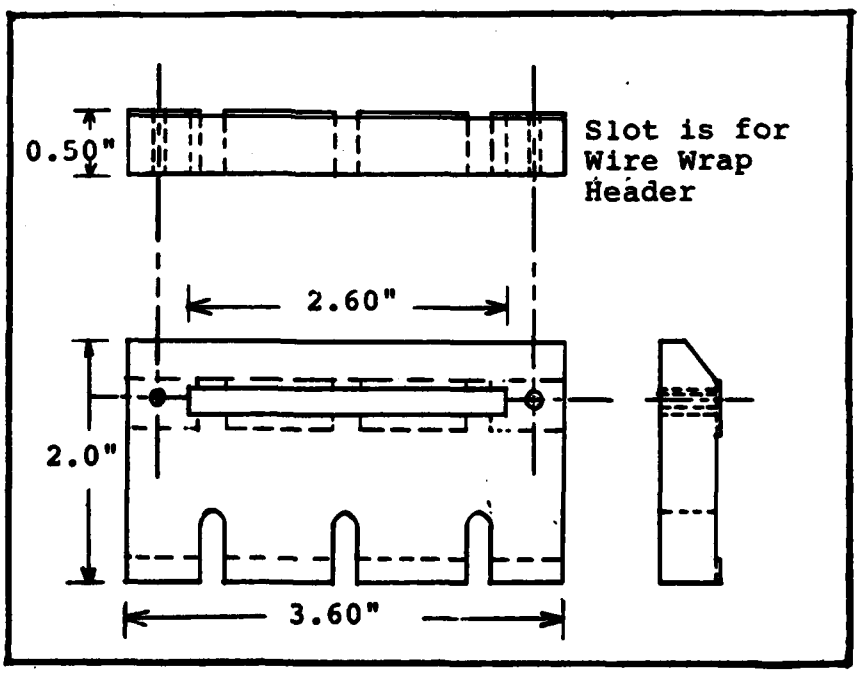

Figure B-3. Wire Wrap Header (Control Line) End Block (Gold Plated Brass)

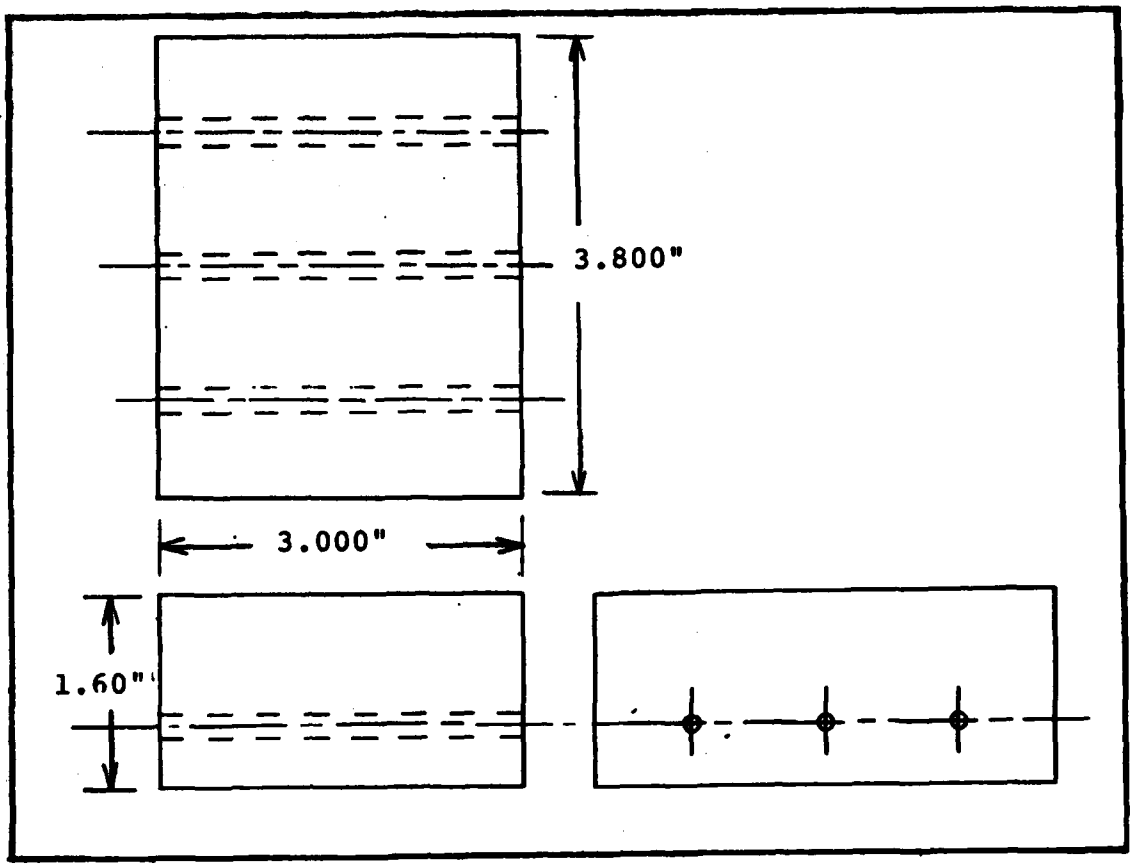

Figure B-4. Base Block for Microwave Fixture (Aluminum)

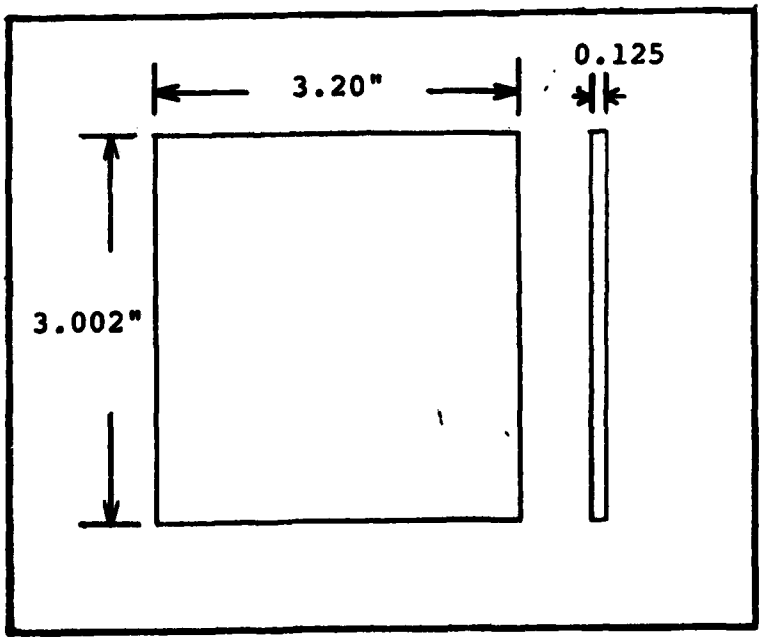

Figure B-5. Ground Plane for Microwave Fixture (Gold Plated Brass)

VITA

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: AFIT/GE/EE/82D-21	2. GOVT ACCESSION NO.: AD-A124 734
3. RECIPIENT'S CATALOG NUMBER:	
4. TITLE (and Subtitle): S-BAND VARIABLE TIME DELAY CIRCUIT ON BARIUM TETRATITANATE	5. TYPE OF REPORT & PERIOD COVERED: MS Thesis
	6. PERFORMING ORG. REPORT NUMBER:
7. AUTHOR(s): Robert F. Bellacicco	8. CONTRACT OR GRANT NUMBER(s):
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Air Force Institute of Technology (AFIT-EN) Wright-Patterson AFB, Ohio 45433	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS:
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (EEAC) Hanscom AFB, Massachusetts 01731	12. REPORT DATE: December 1982
	13. NUMBER OF PAGES: 104
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

Approved for public release: IAW AFR 190-17.

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Dean for Research and Professional Development
Air Force Institute of Technology (ATC)
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4 JAN 1

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Microwave Delay Circuit
Time Delay Circuit
Microstrip
Barium Tetratitanate

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The performance requirements for a variable time delay circuit for use in a phased array antenna are given - time delay from ½ to 16 nsec, 3 GHz operating frequency, 20% bandwidth, tempearture compensation, and compact size. A brief description is presented of various types of devices which could meet these requirements. Microstrip device construction was used in this project.

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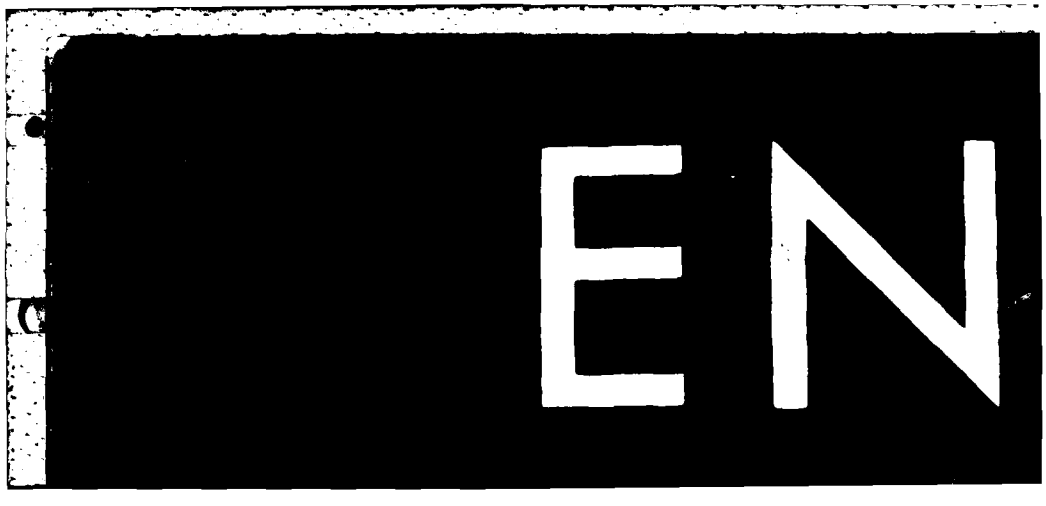
In the research for the electrical structure of this time delay circuit, two design types were investigated. The first, a tapped transmission line, yielded poor results on a test circuit - high insertion loss (2-22 db) and high VSWR. The second design was that of a 5-bit network. Test circuit results showed this to be a relatively good design - insertion loss of 0.7 - 5.0 db and VSWR of 1.8 to 2.5.

A complete time delay circuit design was produced using a 4-bit structure for the RF transmission line (½ to 8 nsec in ½ nsec increments) and a loaded switched-line structure for selection of the amount of time delay. For temperature compensation, the circuit design was dimensioned for a $BaTi_4O_9$ microstrip substrate. Due to small substrate size, the maximum time delay was 8 nsec instead of 16 nsec.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